Analog and Digital CMOS Circuit Design for the Control System of ATLAS Pixel Detector

by

Rizwan Ahmad

Fachhochschule
Dortmund
University of Applied Sciences and Arts

Fakultät für Elektrotechnik und Informatik
Fachhochschule Dortmund
eingebettetes System
Sonnenstrasse 96
44227 Dortmund

Analog and Digital CMOS Circuit Design for the Control System of ATLAS Pixel Detector

Master's Thesis

Submitted to the Electrical Engineering Department
in Partial Fulfillment of the Requirements for the
Degree of

Master of Engineering

by
Rizwan Ahmad

Thesis Supervisor:
Prof. Dr.-Ing. Michael Karagounis
and
M.Eng Andreas Stiller

Dortmund, March 19, 2018

Declaration

(Translation from German)

I hereby declare that I prepared this thesis entirely on my own and have not used outside sources without declaration in the text. Any concepts or quotations applicable to these sources are clearly attributed to them. This thesis has not been submitted in the same or substantially similar version, not even in part, to any other authority for grading and has not been published elsewhere.

Original Declaration Text in German:

Erklärung

Ich versichere, dass ich die Arbeit ohne fremde Hilfe und ohne Benutzung anderer als der angegebenen Quellen angefertigt habe und dass die Arbeit in gleicher oder ähnlicher Form noch keiner anderen Prüfungsbehörde vorgelegen hat und von dieser als Teil einer Prüfungsleistung angenommen worden ist. Alle Ausführungen, die wörtlich oder sinngemäß übernommen worden sind, sind als solche gekennzeichnet.

City, Date

Signature

Abstract

This Master thesis is part of an effort to implement the planned upgrade High-Luminosity Large Hadron Collider (HL-LHC) at CERN Geneva/Switzerland. The ATLAS Pixel Detector which is installed at the LHC is also getting among others a new detector control system (DCS) update. Each module in the Detector Control System will have an integrated DCS chip which includes on-chip shunt and Linear regulators, ADC, bypass transistor and a modified I^2C slave node. In this master thesis, Shunt and Linear regulators are explained and simulated using the Globalfoundaries 130nm CMOS designkit. A Kuijk bandgap reference based Power-On-Reset (POR) circuit is explained and designed in detail. The design of the POR includes an implementation with CMOS instead of diodes or bipolar transistors. It was simulated using Globelfoundaries 130nm CMOS designkit. Finally, a layout was developed for fabrication. The DCS system needs DCS bridge controllers which include a Controller Area Network (CAN) node and a modified I^2C master node. For this purpose CAN and CANopen standards are explained in detail for implementation.

Acknowledgment

- I sincerely express my gratitude and regards for Prof.Dr-Ing. Michael Karagounis for providing me the opportunity to work on this master thesis. During the thesis his supervision was really good and beneficial for me. I sincerely thank him for all the support he gave me from the very first day i started working in this analog and digital design lab.

- I would really like to thank M.Eng Andreas Stiller for helping me out whenever i was stuck with some software or other problems related to lab set-up.

- Special thanks to Mr.Niklaus Lehmann from the University of Wuppertal for helping me out with the layout and simulations and Mr.Alexander Walsemann for providing me a test bench to do a behavioural simulation of the Canakari design.

- I would also like to thank all of my family members and friends for their moral support throughout my education. It is only because of my family especially my father that i could finish things.

Contents

List of Figures

Acronym Description

ASIC	Application Specific Integrated Circuit
DCS	Detector Control System
FET	Field effect transistor
NTC	Negative Temperature Coefficient
PTC	Positive Temperature Coefficient
LDO	Low DropOut
CAN	Controller Area Network
LSB	Least Significant Bit
MSB	Most Significant Bit
POR	Power on Reset
LLC	Logical Link Control
MAC	Medium Access Control
PHS	Physical Signalling
PMA	Physical Medium Attachment
OSI	Open Systems Interconnection
RTR	Remote Transmission Request
Op-Amp	Operational Amplifier
DTMOS	Dynamic Threshold MOSFET
PDO	Process Data Objects
SDO	Service Data Objects
NMT	Network Management Object
ESR	Equivalent Series Resistance
TID	Total Ionizing Dose
STI	Shallow Trench Isolation

1 Introduction

At present different experiments e.g ATLAS[1.1], CMS and ALICE are running at the Large Hadron Collider operated by CERN in Geneva, Switzerland. The ATLAS experiment is working to find out the accurate mass of the Higgs boson particle and other aspects of high energy physics. An upgrade is planned for LHC which requires a new Inner Tracker (ITk)[1.2]. The ATLAS Pixel Detector Control System (DCS) is being developed to prevent overvoltage and overheat damages to the inner pixel detector modules. For this purpose, a DCS chip is being developed in the framework of a collaboration between the University of Wuppertal and Fachhochschule Dortmund [3].

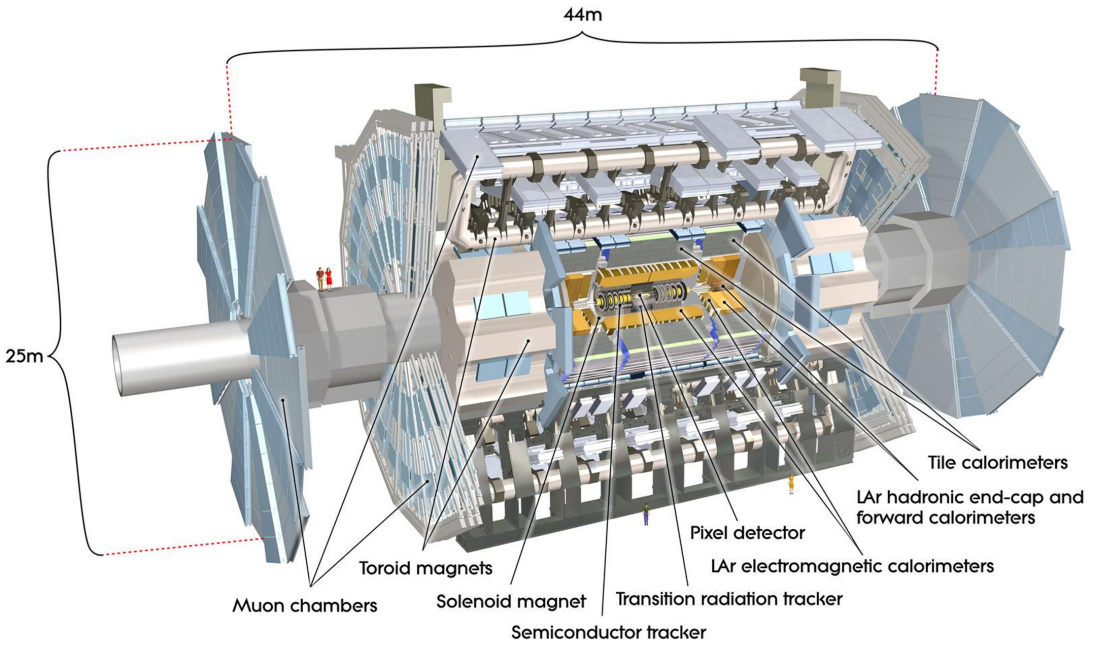

Figure 1.1: ATLAS Pixel Detector

The DCS consists of three main parts. As shown in figure 1.3 it consists of a DCS Computer, DCS Controller and DCS Chip.

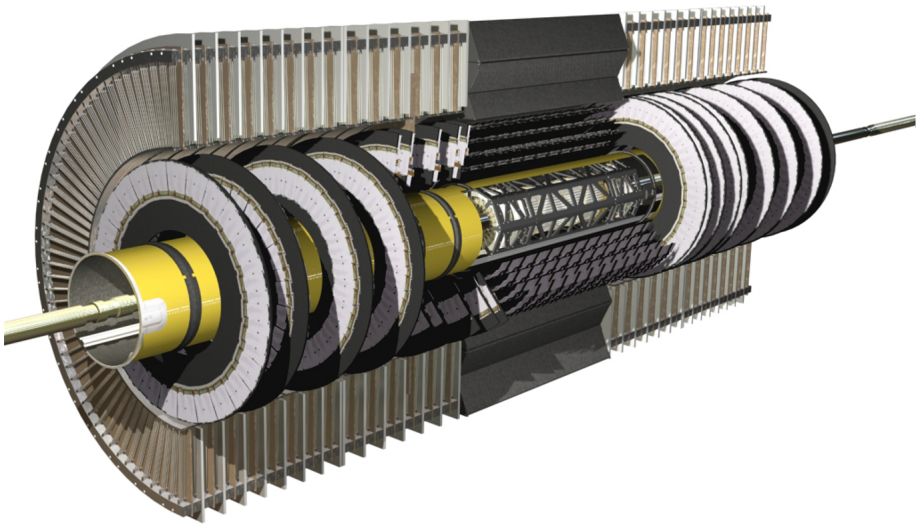

Figure 1.2: Inner Detector

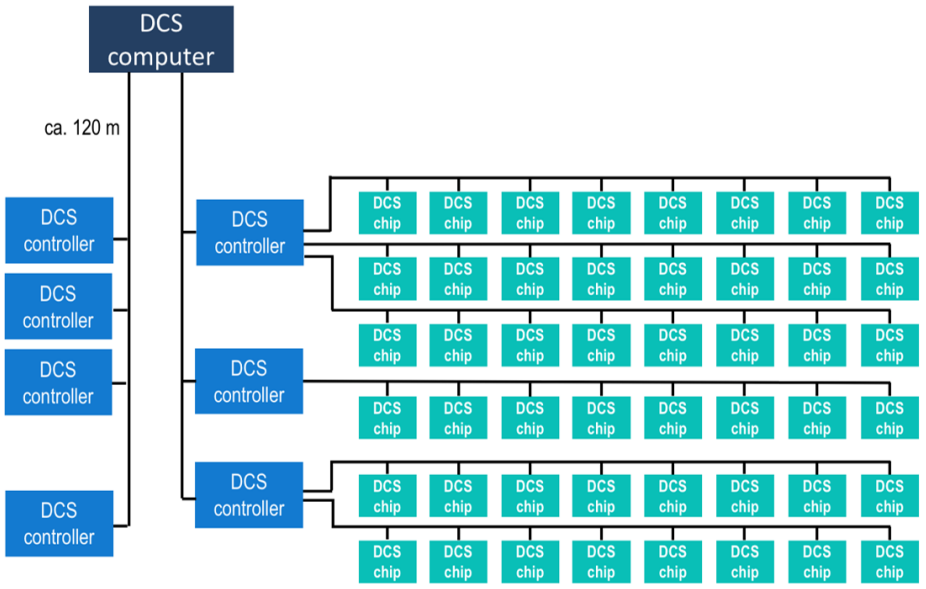

Figure 1.3: Detector Control System (DCS)

DCS Computer

The DCS Computer is the central control server which operates and communicates with all the inner pixel detector modules via the DCS chip. It can autonomously switch off any module which is damaged or creating troubles. The DCS computer collects all the DCS related data from ATLAS Pixel Detector and can configure each module.

DCS Controller

The DCS Controller act as a bridge between DCS chip and DCS computer. It has an integrated CAN node and a modified I^2C master on the same chip and must be radiation hard. This DCS Controller can be hardwired bridge logic between CAN node and modified I2C master or it can also be a microcontroller which can be programmed for the required communication protocol. The DCS Controller receives data via a CAN bus from the DCS computer and distributes information to each module using a modified I^2C master node. Each module then has a DCS slave on it.

DCS chip

The DCS chip is attached to each inner pixel detector module and can bypass any faulty module to prevent collapse of the whole system. This chip is fabricated on a 130nm CMOS technology, it includes integrated regulators, Power on Reset, ADC, Power switch and I^2C slave. Each DCS chip is monitored and controlled from the DCS Computer. This chip has already been designed by the joint collaboration of FH Dortmund and the University of Wuppertal.

1.1 Motivation

The DCS system has to be adapted to the new powering scheme of the ATLAS Pixel Detector which is based on a current supply which feeds a chain of serial-connected modules shown in figure 1.4. These modules have all a different local ground potential which varies depending upon the number of modules in one chain, while the DCS chip is only able to sustain a voltage drop smaller than 2.5V. Assuming the maximum module voltage of 2V across each module, the minimum and maximum ground potential will be 10V to 40V respectively [4]. To

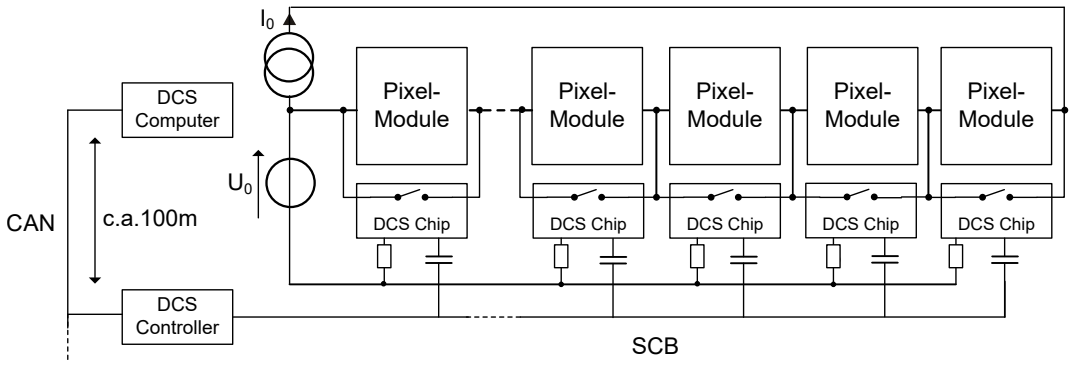

Figure 1.4: Detector Control System (DCS) serial powering

solve this challenge resistors are placed between the voltage source (V_{DCS}) and the shunt regulator integrated into each DCS chips. The value of this resistor can be calculated by using the following relation:

$$R_{PWR} = \frac{V_{DCS} - V_{LOCALGND}}{I_{SUP}} \tag{1.1}$$

Where V_{DCS} is supply voltage which supplies the DCS system with 15V for a chain of 5 modules and 45V for a chain of 16 modules [4]. While the integrated shunt regulator generates an output voltage of 2.3V the remaining voltage fraction drops across the R_{PWR}. The output of the shunt regulator is then fed into the Linear regulator which generate supply voltages for the analog and digital part of the chip. The next task is to design a Power-On-Reset circuit that was missing in the previous iteration of the chip which is very important to ensure that system starts in a known state i.e. all the flipflops are reset and the system does not go into race conditions. For the DCS Controller an already built CAN protocol unit is available but it needs to be analysed and verified. For this purpose, CAN standard must be learned. Also, the CANopen standard is required in the future for communication at the application layer.

1.2 Objective

This master thesis is divided mainly into three parts.

1. Shunt and Linear Voltage Regulators

2. Power-On-Reset circuit

3. CAN and CANopen standard to analyse CAN node.

Main tasks are to design a shunt regulator with the output voltage of 2.3V and by running corner simulations to make sure it works in all conditions e.g. load, line regulation, startup, stability etc. Three different linear regulators are needed with output voltages of 1.0,1.2 and 1.5V for the analog and digital logic on the chip. For the chip, a Power-On-Reset circuit needs to be designed which releases the reset when the power supply is stabilized and reaches a certain threshold. In this circuit the requirement is to release the reset at a minimum voltage 950 mV. CAN standard ISO 11898:2015 must be learned to analyse already implemented CAN node and also CANopen standard must be learned to check how it can be implemented at the application layer for the same node.

2 Theoretical Design Concepts and Literature Review

This chapter is divided into three main parts.

- Regulators
  - Shunt Regulator
  - Linear Regulator
- Power-On-Reset Circuit
- CAN ISO 2015:11898 and CANopen Standard

2.1 Regulators

There are different topologies of regulators for on-chip power management. We are interested here in shunt and linear regulators. Some general parameters to characterise voltage regulators are mentioned below:

Quiescent Current

Quiescent current is defined as the difference between the input current and the output current.

$$I_Q = I_{IN} - I_{LOAD} \tag{2.1}$$

which in turn affects the actual power delivered to the load with respect to input power. All of the internal components contribute towards quiescent current. Because of this reason, shunt regulators are not very power efficient [5].

Power Supply Rejection Ratio

Power Supply Rejection Ratio (PSRR) is the parameter of voltage regulators which describes the ability of a voltage regulator to keep its output voltage constant when the input voltage is fluctuating. It is frequency dependent [6].

$$PSRR = \frac{V_{OUT}}{V_{IN}} \tag{2.2}$$

Load Regulation

Load regulation is the parameter that defines how well the regulator is able to keep its output voltage constant when the load current changes [6].

$$Load\,Regulation = \frac{\Delta V_{OUT}}{\Delta I_{OUT}}.100\% \tag{2.3}$$

Temperature Dependence

Voltage regulators are sensitive to changes in the operating temperature. This temperature dependence comes from two sources, one is temperature dependence offset of the error amplifier and rest is the bandgap reference circuit [6].

$$Temperature\,Dependence\,Parameter = \frac{\Delta V_{OUT}}{\Delta T} \tag{2.4}$$

Line Regulation

Line regulation defines the ability of a voltage regulator to keep its output voltage constant with respect to change in the input voltage [7].

$$Line\,Regulation = \frac{\Delta V_{OUT}}{\Delta V_{IN}}.100\% \tag{2.5}$$

Power Efficiency

The power efficiency of the voltage regulators is defined as output power divided by the input power. The power efficiency of regulators can never reach 100% due to the fact that there is quiescent current in Linear regulators and shunt path current in shunt regulators [6].

$$Power\,Efficiency = \frac{P_{OUT}}{P_{IN}} \tag{2.6}$$

2.1.1 Shunt Regulator

In a shunt regulator, the load is connected in parallel to the shunt element. For each DCS chip in the ATLAS Pixel Detector, the shunt regulator is needed to operate in a serial chain. A constant current is provided as the excess current which is not required for the operation is passed through the shunt element [8] [4]. It can be seen in figure 2.1 a very simple shunt regulator can be made by just placing a Zener diode in parallel to the load. A forward biased zener diode behaves just like a simple diode. This zener diode can be reverse biased until it reaches a point called Avalanche breakdown region. Beyond this point increasing the current does not affect voltage and it remains constant. This Zener diode is operated in the reverse Zener breakdown region. If the supply voltage is increased from the nominal value this causes an increase in the supply current. Looking at the Zener diode characteristics we can see that when it is operated in the reverse breakdown down region this extra current is bypassed through a Zener diode keeping the current and a voltage constant at the load. In the other scenario if the load current increases this causes a decrease in the Zener diode current but the voltage is still kept constant. This topology is very simple and works for simple and small circuits [9].

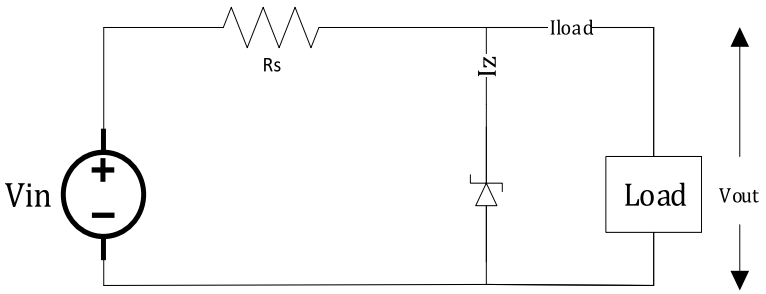

Figure 2.1: Zener diode regulator

In this project, another topology is employed using an operational amplifier in the negative feedback configuration to minimize power consumption and for better stability, performance and load/line regulation of the system which is shown in figure 2.2. In this circuit, the operational amplifier is fed with a reference and a feedback from the output. It then calculates the difference between the two and

increase/decrease the shunt current through the shunt element to regulate the output voltage.

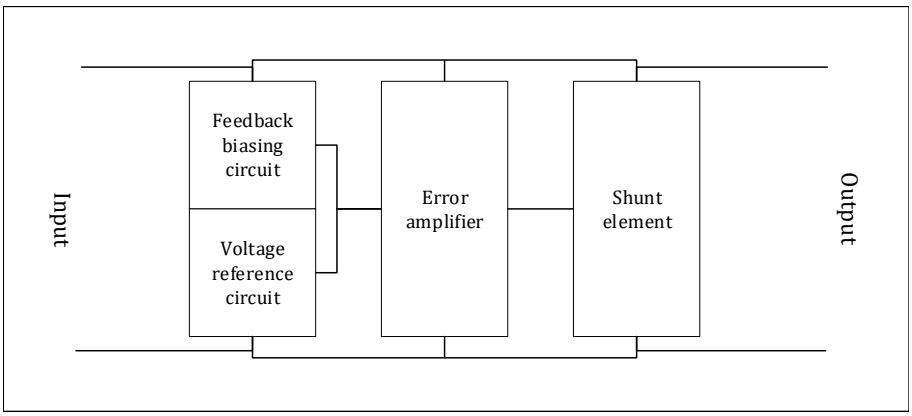

Figure 2.2: Shunt regulator

2.1.2 Linear Voltage Regulators

Linear regulators are of basically two types.

- Basic Type
- LDO Type

The basic type of linear regulators is more stable but need a large difference between the input voltage and the output voltage for proper regulation so their dropout voltage is high. Also they do not need an output capacitance to achieve stability. Basic linear regulators use mostly bipolar transistors as pass element that is also one of the reason for high current consumption [5]. Low dropout regulators are much more power efficient. They need very little difference between the input and the output voltage for proper regulation [5]. Linear voltage regulators are step down devices. They use the voltage controlled current source to output a constant voltage output. A linear regulator has 4 main components namely a voltage reference, an error amplifier, a pass element and a sampling network shown in figure 2.3. The working principle of a linear regulator is rather simple. It consists of a feedback loop. The output is compared to a reference by an error amplifier. The difference is then used to control a pass device which is actually a voltage controlled current device. So in this way by controlling the gate-source voltage, the current going through the pass element can be controlled which in

turn controls the output voltage [6]. The pass element for the Linear regulator can be an n-channel device or a p-channel device. A brief description is mentioned below for both of them.

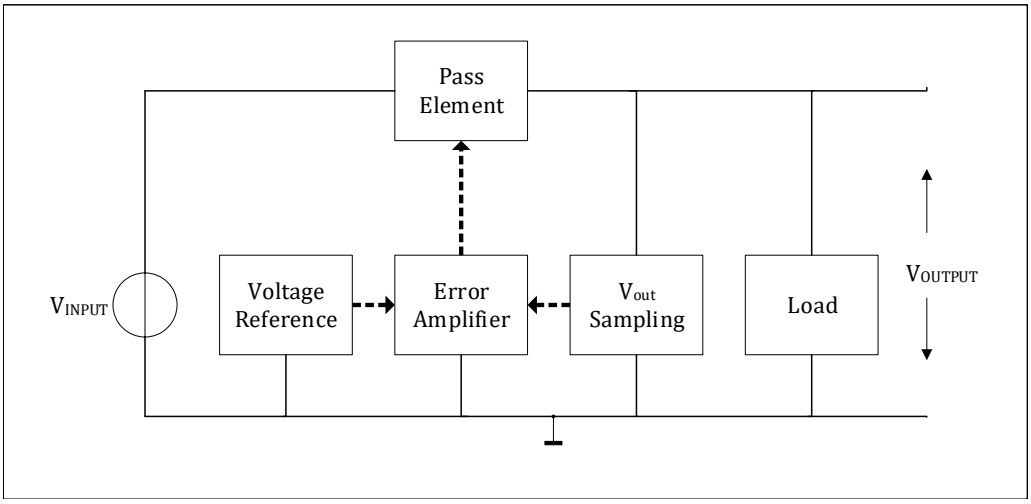

Figure 2.3: Linear regulator block

N-channel pass element

The N-channel pass device is connected in common drain configuration. Because of common drain configuration it exhibits very low output impedance which makes it much more stable. In the normal operation mode NMOS also exhibits lower resistance as compared to PMOS pass device. The dropout voltage for n-channel devices can be very high [6]. In this master thesis, a linear voltage regulator with N-channel pass device is implemented. which is shown in figure 2.4.

P-channel pass element

When a p-channel device is used as a pass element, it is connected in common source configuration and acts as an additional amplification stage. In this way an additional -90 degrees phase shift is automatically added to the output which makes it much more unstable. An external capacitor is then required to make it stable. We need to introduce a zero which gives +90 degrees phase shift. This zero can be placed by using an external capacitance with high equivalent series resistance (ESR) which also gives an additional benefit of filtration.

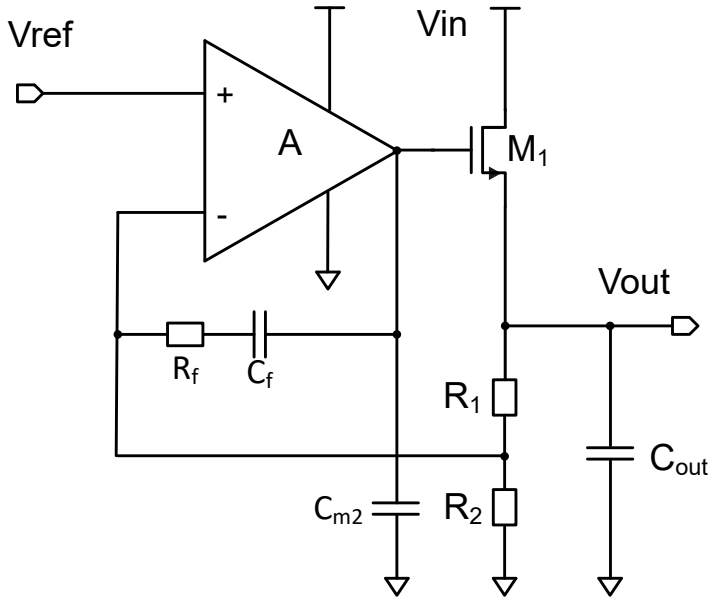

Figure 2.4: Linear regulator

Figure 2.4 shows the implementation of the linear regulator with the NMOS pass device.

Linear regulator small signal analysis for Load/Line regulation and the reference voltage

Small signal equivalent circuit for the Linear regulator with the NMOS pass element (figure 2.4) is shown in figure 2.5.

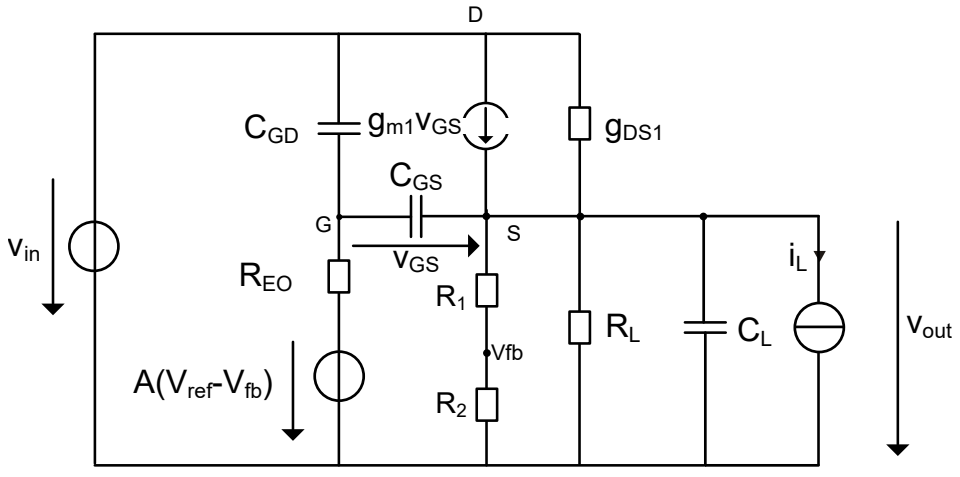

Figure 2.5: Linear small signal equivalent circuit

In order to do static analysis, this circuit can be further simplified by removing all capacitances and the output impedance R_{EO} of the error amplifier. In addition, the equivalent load resistance at the regulator output has been calculated taking account of R_2 and R_L to be:

$$R_G = (R_1 + R_2) \,||R_L \tag{2.7}$$

In addition taking into account that the feedback voltage V_{fb} is the series voltage drop across resistor R_2. V_{fb} can be calculated by the following equation:

$$V_{fb} = \beta V_{out} \tag{2.8}$$

Where

$$\beta = \frac{R_2}{R_1 + R_2} \tag{2.9}$$

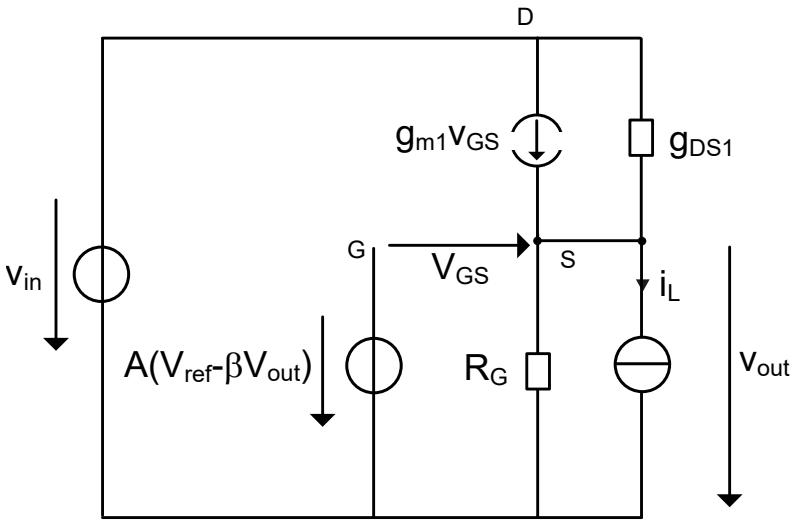

Figure 2.6: Linear small signal equivalent circuit for static analysis

By applying modified nodal analysis [10] to the circuit shown in figure 2.6 we can write a system of equations.

$$\begin{pmatrix} g_{DS1} & -g_{DS1} & 0 & -1 & 0 \\ -g_{DS1} & g_{DS1}+G_G & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \end{pmatrix} . \begin{pmatrix} v_D \\ v_S \\ v_G \\ i_D \\ i_G \end{pmatrix} = \begin{pmatrix} -g_m v_{GS} \\ -g_m v_{GS} - i_L \\ 0 \\ V_{in} \\ A(V_{ref} - \beta v_S) \end{pmatrix}$$

Considering the mapping of the gate-source voltage and the output voltage to node potential of the circuit $v_{GS} = v_G - v_S$ and $v_S = v_{out}$. The equation system can be modified to:

$$\begin{pmatrix} g_{DS1} & -g_{DS1} & 0 & -1 & 0 \\ -g_{DS1} & g_{DS1}+G_G & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \end{pmatrix} . \begin{pmatrix} v_D \\ v_S \\ v_G \\ i_D \\ i_G \end{pmatrix} = \begin{pmatrix} -g_m v_G + g_m v_S \\ g_m v_G - g_m v_S - i_L \\ 0 \\ V_{in} \\ AV_{ref} - A\beta v_S \end{pmatrix}$$

$$\begin{pmatrix} g_{DS1} & -g_{DS1}-g_m & g_m & -1 & 0 \\ -g_{DS1} & g_{DS1}+G_G+g_m & -g_m & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & A\beta & 1 & 0 & 0 \end{pmatrix} . \begin{pmatrix} v_D \\ v_S \\ v_G \\ i_D \\ i_G \end{pmatrix} = \begin{pmatrix} 0 \\ -i_L \\ 0 \\ V_{in} \\ AV_{ref} \end{pmatrix}$$

Now using Cramer's rule, the value of v_S can be calculated in terms of the reference voltage, load current and input voltage.

$$v_S = \frac{\begin{vmatrix} g_{DS1} & 0 & g_m & -1 & 0 \\ -g_{DS1} & -i_L & -g_m & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 \\ 1 & V_{in} & 0 & 0 & 0 \\ 0 & AV_{ref} & 1 & 0 & 0 \end{vmatrix}}{\begin{vmatrix} g_{DS1} & -g_{DS1} - g_m & g_m & -1 & 0 \\ -g_{DS1} & g_{DS1} + G_G + g_m & -g_m & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & A\beta & 1 & 0 & 0 \end{vmatrix}}$$

Now using Laplace expansion method we can find both determinants so that upper system of equations reduces to:

$$v_S = \frac{g_{DS1}V_{in} + g_m AV_{ref} - i_L}{g_{DS1} + g_m + G_G + A\beta g_m} \tag{2.10}$$

Which can also be written as:

$$\begin{aligned} v_S = \left(\frac{g_{DS1}}{g_{DS1} + g_m + G_G + A\beta g_m}\right) V_{in} + \left(\frac{g_m A}{g_{DS1} + g_m + G_G + A\beta g_m}\right) V_{ref} \\ - \left(\frac{1}{g_{DS1} + g_m + G_G + A\beta g_m}\right) i_L \end{aligned} \tag{2.11}$$

Assuming $A\beta g_m >> g_{DS1} + g_m + G_G$. Equation 2.11 reduces to:

$$v_S \approx \left(\frac{g_{DS1}}{A\beta g_m}\right) V_{in} + \left(\frac{1}{\beta}\right) V_{ref} - \left(\frac{1}{A\beta g_m}\right) i_L \tag{2.12}$$

Line regulation is then given by:

$$\frac{v_S}{V_{in}} = \left(\frac{g_{DS1}}{A\beta g_m}\right) \tag{2.13}$$

Load regulation is given by:

$$\frac{v_S}{i_L} = -\left(\frac{1}{A\beta g_m}\right) \tag{2.14}$$

In addition, the output voltage as a function of the reference voltage can be calculated as:

$$\frac{v_S}{V_{ref}} = \left(\frac{1}{\beta}\right) \quad or \quad \frac{v_S}{V_{ref}} = \left(\frac{R_1 + R_2}{R_2}\right) \tag{2.15}$$

Linear regulator

For the better understanding of the regulator circuit operation, the error amplifier is analysed separately. The error amplifier together with its feedback and input circuitry is shown in figure 2.4. For simplification the reference voltage at the non inverting input has been replaced by a short to ground.

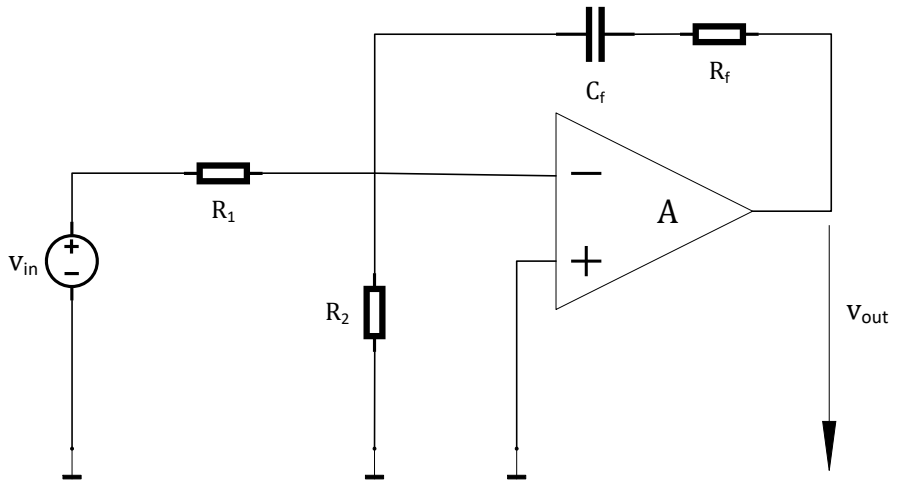

Figure 2.7: Linear regulator circuit for transfer function calculation

For simplification, elements are replaced with equivalent impedances in figure 2.8.

$$Z_2 = R_f + \frac{1}{sC_f} \quad and \quad Z_1 = R_2||R_1 \tag{2.16}$$

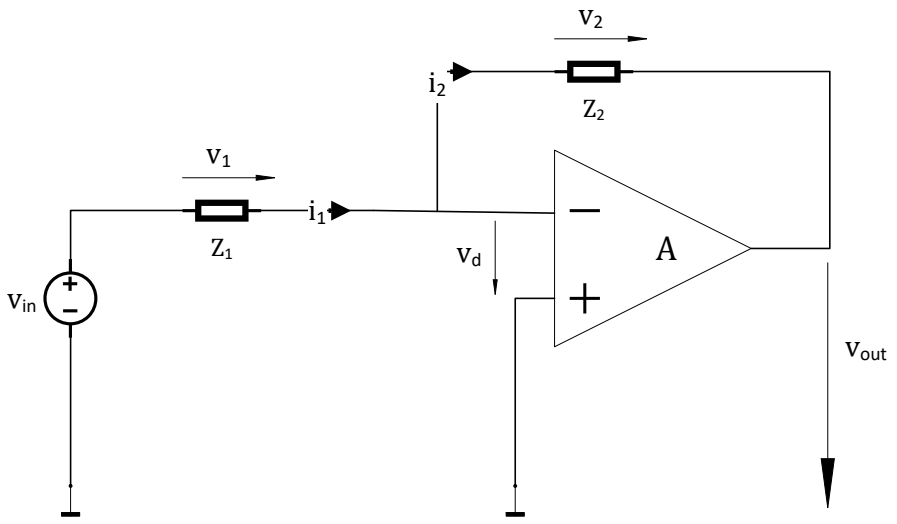

Figure 2.8: Linear regulator simplified circuit for transfer function calculation

From figure 2.8, taking into account the high input impedance of the error amplifier the input current i_1 is equal to the current in the feedback path.

$$i_1 = i_2 \tag{2.17}$$

Applying ohms law gives:

$$\frac{v_1}{z_1} = \frac{v_2}{z_2} \tag{2.18}$$

Introducing the relationship between v_1, v_{in} and v_d respectively v_2,v_d and v_{out} by a mesh equation, the equation can be modified to be:

$$\frac{v_{in} - v_d}{z_1} = \frac{v_d - v_{out}}{z_2} \tag{2.19}$$

$$\frac{v_{in}}{z_1} + \frac{v_{out}}{z_2} = \left(\frac{1}{z_1} + \frac{1}{z_2}\right) v_d \tag{2.20}$$

The voltage difference at the amplifier input is amplified to give the output voltage.

$$v_{out} = -Av_d \tag{2.21}$$

$$v_d = \frac{-v_{out}}{A} \tag{2.22}$$

$$\frac{v_{out}}{v_{in}} = -\frac{\dfrac{z_2}{z_1+z_2}}{\dfrac{z_1}{z_1+z_2}+\dfrac{1}{A}} \tag{2.23}$$

$$\frac{v_{out}}{v_{in}} = -\frac{\dfrac{z_2}{z_1}}{1+\left(1+\dfrac{z_2}{z_1}\right)\dfrac{1}{A}} \tag{2.24}$$

If $A \to \infty$ then $v_{out} = -\dfrac{z_2}{z_1}v_{in}$

Equation 2.24 can be re-written as:

$$H(s) = -\frac{A\dfrac{z_2}{z_1}}{A+\left(1+\dfrac{z_2}{z_1}\right)} \tag{2.25}$$

Replacing original values of the z_1 and the z_2 in equation 2.25:

$$H(s) = -\frac{A\left(\dfrac{1+sR_fC_f}{sC_f(R_1||R_2)}\right)}{A+\left(1+\dfrac{1+sR_fC_f}{sC_f(R_1||R_2)}\right)} \tag{2.26}$$

Simplifying 2.26 the following result is derived:

$$H(s) = -\frac{(1+sR_fC_f)A}{1+s\left((1+A)C_f(R_1||R_2)+R_fC_f\right)} \tag{2.27}$$

Analysing the equation 2.27, there are one pole and one zero in the transfer function. This pole is the dominant pole which defines the 3db cut-off frequency of the regulator circuit open-loop transfer function. Assuming the gain A of the amplifier to be very high. The term R_fC_f in the denominator can be ignored. This pole is compensated by the zero and after that the amplifier has a constant gain.

Equation 2.27 reduces to:

$$H(s) = -\frac{R_f}{R_1||R_2} \tag{2.28}$$

NMOS pass element frequency response

For the complete loop gain calculation the frequency behaviour of the NMOS behaviour has to be derived. Figure 2.9 shows the small signal equivalent circuit for the NMOS pass element.

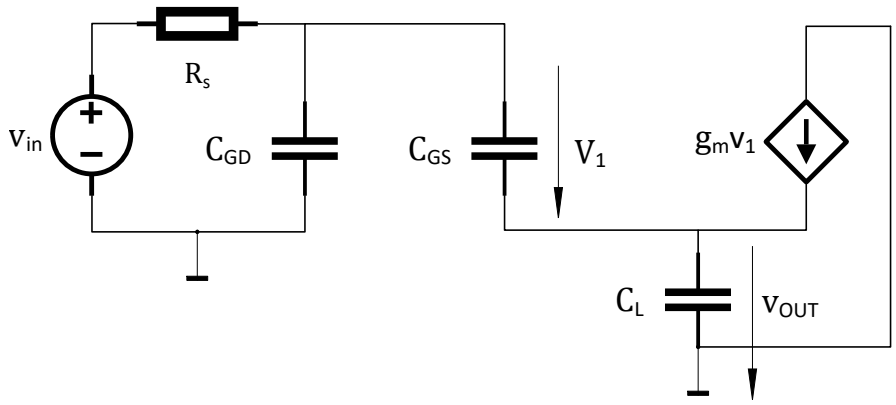

Figure 2.9: Source follower high frequency equivalent circuit

Applying KCL to the output node shown in figure 2.9 gives:

$$sv_1C_{GS} + g_m v_1 = v_{out}C_L s \tag{2.29}$$

$$v_1 = \left(\frac{C_L s}{g_m + sC_{GS}}\right) V_{out} \tag{2.30}$$

Now by applying KVL,

$$v_{in} = R_s(v_1 C_{GS} s + (v_1 + v_{out})C_{GD} s) + v_1 + V_{out} \tag{2.31}$$

Substituting the value of v_1 into the equation 2.31, the transfer function can be written as:

$$\frac{v_{out}}{v_{in}} = \frac{g_m + C_{GS}s}{R_s(C_{GS}C_L + C_{GS}C_{GD} + C_{GD}C_L)s^2 + (g_m R_s C_{GD} + C_L + C_{GS})s + g_m} \tag{2.32}$$

Two poles are added into the system because of the input capacitance (gate-source and gate-drain) and the load capacitance. The system has one zero in the left half plane.

These poles are very near to each other which causes an abrupt phase shift of 180°. A capacitance is added between the output of the amplifier and ground as shown in figure 3.7 to separate these poles. By adding an additional capacitor one of the poles goes to lower frequency such that the gain is already less than 0db when the second pole starts acting. By placing the low frequency pole of the NMOS pass device close to the zero introduced by the error amplifier feedback elements the required phase margin is achieved. For further reading please refer to [11].

2.2 Power-On-Reset Circuit

A circuit which detects an applied input power supply to pass a reset signal to the supplied circuit or system until the supply voltage reaches a specified threshold is called a Power-on-Reset (POR) circuit. This circuit makes sure that all digital logic circuit elements i.e. flipflops and latches start in a known state excluding undesirable behaviour or race conditions. When the power is applied it takes some transitional time after which the voltage gets to the required stabilized value. Assuming an integrated circuit which operates correctly at 1V. During the ramp of the power supply voltage a little bit of time will be consumed until the supply voltage reaches 1V so during this period of time a circuit which applies a reset so that all the latches and flipflops start in a uniform known state for correct behaviour. This POR circuit must release the reset when the supply voltage is close to 1V. Different topologies are possible for POR circuits but in this master thesis a process and temperature tolerant bandgap reference based POR is implemented. The concept of this POR circuit is taken from [2] and Core of this POR circuit is bandgap reference proposed in [1] which is shown in figure 2.13.

The working principle of this POR circuit is described in two parts. First, the bandgap reference circuit is explained briefly and after that the comparator circuit is discussed. A block diagram can be seen in figure 2.10. A temperature and process independent reference voltage is generated by a bandgap circuit which is then fed into the comparator. The comparator then looks for the crossing point of two voltages which have a positive (PTC) or negative temperature coefficient (NTC) respectively. At that crossing point the reset is released.

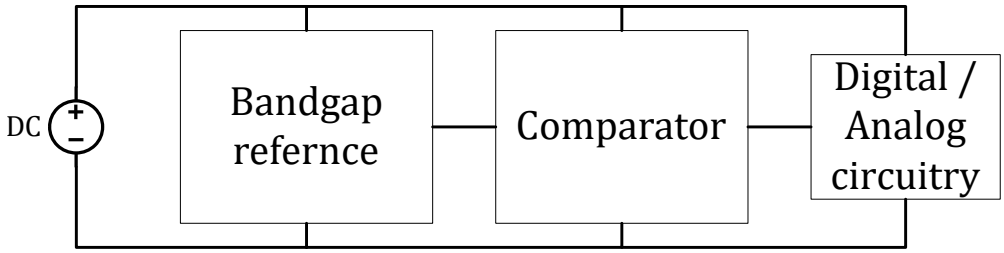

Figure 2.10: Power on reset block diagram

2.2.1 Bandgap Reference

All of the regulators in the DCS chips and the POR circuit also require a reference voltage source which should be independent of temperature and process variation. A reference voltage source independent of temperature variation generally is also independent of process variation. For further reading please refer to [11].

Voltage reference circuits can be implemented in many different ways [12].

1. Diode/Bipolar transistors
2. MOS transistors in weak inversion
3. MOS transistors in weak inversion with forward biased junction diode DT-MOS

Diode/Bipolar based bandgaps are very accurate and less dependent on process corner but are susceptible to radiation. Hence the reference varies with radiation dose.
MOS transistor based bandgaps are radiation hard but depend very strongly on process corner and require trimming.
Dynamic Threshold MOSFET (DTMOS) transistor based bandgaps are also radiation hard but depend to a lesser extent on process corner than regular MOS transistor based bandgap circuits [13].

Negative Temperature Coefficient NTC

A negative temperature coefficient in the framework of the bandgap circuit means that the voltage dropping across a particular device decreases with increasing

temperature. Bipolar transistors exhibit negative temperature coefficient at the base-emitter voltage when their base emitter junction is forward biased or in other words we can also say that a PN junction diode in forward biased condition is a NTC device. The forward biased characteristics graph of the diode in the first quadrant moves to the left. The effective threshold voltage is decreased.

A Current of a PN junction diode in the forward biased condition or the bipolar transistor can be written as [11]:

$$I_c = I_s \exp \frac{V_{BE}}{V_T} \tag{2.33}$$

In this equation

V_T is the temperature voltage which is equal to $k\frac{T}{q}$.
I_S is the saturation current which is proportional to $\mu k T {n_i}^2$.
μ is the mobility of minority carriers and n_i is the intrinsic minority carrier. Both μ and n_i are temperature dependent quantities.

$$\mu \propto \mu_0 T^m \qquad with \qquad m \approx \frac{-3}{2} \tag{2.34}$$

while

$${n_i}^2 \propto T^3 \exp \frac{-E_g}{kT} \qquad with \qquad E_g \approx 1.12eV \tag{2.35}$$

So , the saturation current will be

$$I_s = bT^{4+m} \exp \frac{-E_g}{kT} \tag{2.36}$$

To find the variation of V_{BE} with respect to temperature we can take the partial derivative of base emitter voltage which is

$$V_{BE} = V_T \ln \frac{I_C}{I_S} \tag{2.37}$$

Partial derivative with respect to the temperature will be

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} \ln \frac{I_C}{I_S} - \frac{V_T}{I_S} \frac{\partial I_S}{\partial T} \tag{2.38}$$

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4+m)V_T - \frac{E_g}{q}}{T} \tag{2.39}$$

With $V_{BE} \approx 750mV$ and $T = 300K$ equation 2.39 gives us the negative temperature coefficient of $\approx -1.5\frac{mV}{K}$ [11].

Positive Temperature Coefficient PTC

Positive temperature coefficient means that the effective resistance of any component or material increases with the increase in temperature e.g. thermistors. PTC components are self limiting due to the fact that their resistance increases with the increase in temperature.

Temperature Independence

So, to cope with the NTC of bipolar transistors or PN diodes we need to introduce equal amount of PTC to get temperature independent voltage reference. This PTC can be introduced with the help of two bipolar transistors operating at different current densities [14]. If we consider the transistors to be ideal and having equal base currents then the difference between their base emitter voltages is a PTC voltage. which can be then added to NTC voltage to cancel its effect. Diagram depicting the fundamental concept is shown in figure 2.11.

$$\Delta V_{BE} = V_{BEQ2} - V_{BEQ1} \tag{2.40}$$

$$\Delta V_{BE} = V_T \ln \frac{nI_0}{I_{S2}} - V_T \ln \frac{I_0}{I_{S1}} \tag{2.41}$$

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} \ln n \tag{2.42}$$

n is the difference in current density. Here base and collector are shorted for both transistors Q_1 and Q_2 in this way they just behave like a forward biased PN junction diode having a voltage drop of V_{BE}. when we take the difference of these two voltages the resultant has a positive temperature coefficient. Equation 2.42 has a positive temperature coefficient. In figure 2.11 in place of one transistor Q_1 we can use multiple transistors in parallel to increase the log factor. If we use more than one transistors then equation 2.41 becomes

$$\Delta V_{BE} = V_T \ln \frac{nI_0}{I_{S2}} - V_T \ln \frac{I_0}{mI_{S1}} \tag{2.43}$$

where m is the number of transistors. Equation 2.42 then can be written as

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} \ln(nm) \quad or \quad V_T \ln(nm) \tag{2.44}$$

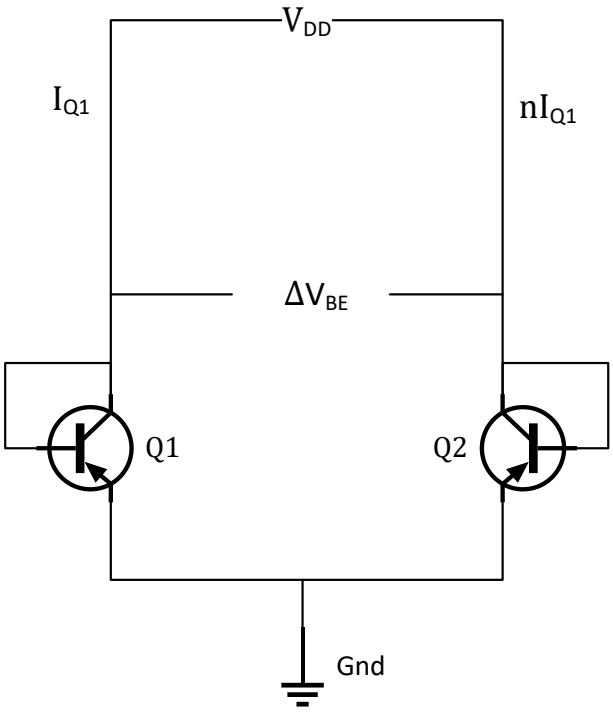

Figure 2.11: Positive temperature coefficient generation

By using the concepts of positive and negative temperature coefficient voltages a voltage reference circuit can be developed. which is independent of temperature variation or has a zero temperature coefficient. However a specific implementation technique is required to superimpose PTC voltage calculated in equation 2.42 to V_{BE} and to identify the value of difference in current densities or number of transistors which is required to get exactly $\approx +1.5\frac{mV}{K}$ to cancel NTC.

Assuming that the generated reference voltage can be described by the following equation

$$V_{REF} = \alpha_1 V_{BE} + \alpha_2 (V_t \ln n) \tag{2.45}$$

Where $V_t \ln n$ is the PTC voltage which results the difference of base emitter

voltages. Then the values of α_1 and α_2 can calculated as explained below:

At room temperature equation 2.45 gives us $\frac{\partial V_{BE}}{\partial T} \approx \frac{-1.5mV}{K}$ and $\frac{\partial V_T}{\partial T} \approx \frac{+0.087mV}{K}$

if we suppose $\alpha_1 = 1$ and α_2 in such a way that $(\alpha_2 \ln n)(0.087\frac{mV}{K}) = 1.5\frac{mV}{K}$ then in such case $\alpha_2 \ln n \approx 17.2$

Equation 2.45 then can be written as

$$V_{REF} \approx V_{BE} + 17.2V_T \approx 1.25 \tag{2.46}$$

To add the NTC and the PTC which are V_{BE} and $17.2V_T$ respectively. As shown in figure 2.12 if the voltages V_1 and V_2 are equalized then the voltage across resistor R will be

$$V_R = V_{BE1} - V_{BE2} = V_T \ln n \tag{2.47}$$

Which is positive coefficient. In such a case V_2 becomes

$$V_2 = V_{BE2} + V_T \ln n \tag{2.48}$$

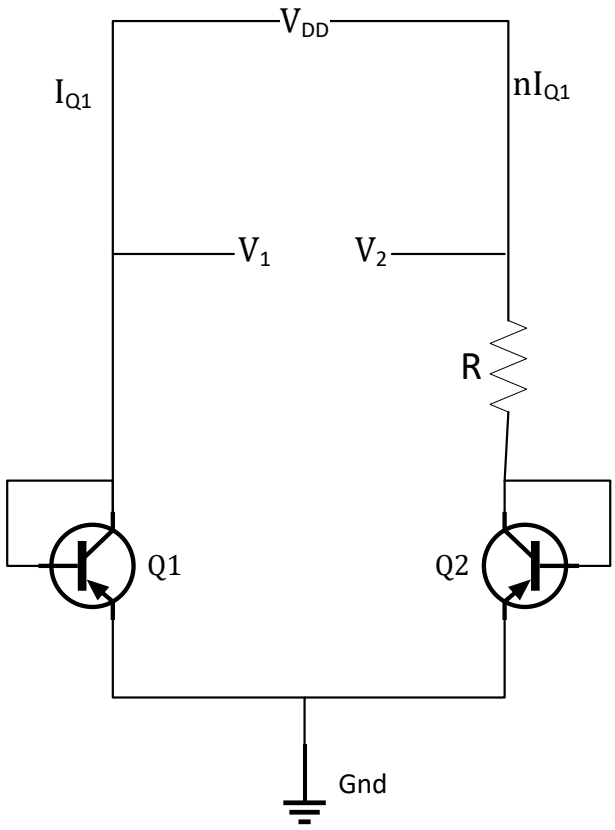

Figure 2.12: Temperature independent voltage generation

To make the circuit in figure 2.12 work two conditions must be satisfied which are mentioned below:

- Equalization of V_1 and V_2
- Setting the term $\alpha \ln n$ to the value of ≈ 17.2 we can scale it by choosing proper resistor and the current

As shown in figure 2.13 an operational amplifier is employed in order to fulfil both of these conditions. In addition bipolar transistors connected in diode configuration can be also be replaced by PN junction diodes.

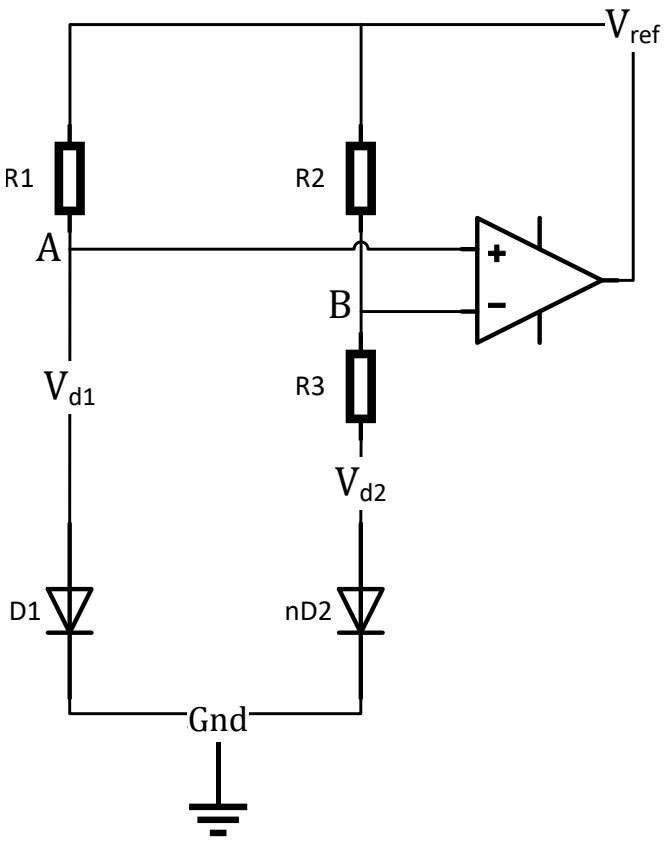

Figure 2.13: Kuijk cell bandgap reference [1]

In figure 2.13, R_1 and R_2 are kept equal in order to make sure that the voltages at point A and B are approximately equal. Analysing the opamp circuit we assume a virtual short circuit between the inverting and the noninverting opamp input giving rise to voltages at points A and B of same value. As a result voltage at point B will be V_{d1} and the voltage across R_3 will be

$$V_{d1} - V_{d2} = V_T \ln n \tag{2.49}$$

V_{REF} will be then

$$V_{REF} = V_{d2} + \frac{V_T \ln n}{R_3}(R_3 + R_2) \tag{2.50}$$

$$V_{REF} = V_{d2} + (V_T \ln n)\Big(1 + \frac{R_2}{R_3}\Big) \tag{2.51}$$

or in other words it can also be written as [2]

$$V_{REF} = V_{d1} + R_2 * I_{ptat} \tag{2.52}$$

where I_{ptat} is shown in figure 2.14.

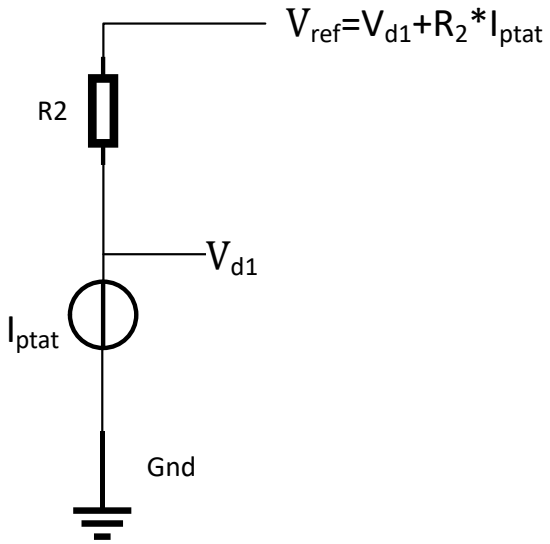

Figure 2.14: Current proportional to absolute temperature

2.2.2 Comparator

Basic theoretical concepts of comparator circuit are taken from [15]. Voltage comparator circuits belong to the family of *nonlinear analog circuits* because the inputs and outputs are not related to each other in a linear fashion. These circuits are classified as neither purely analog nor purely digital.

Core Concepts

A very basic concept of the comparator circuit is shown in figure 2.15

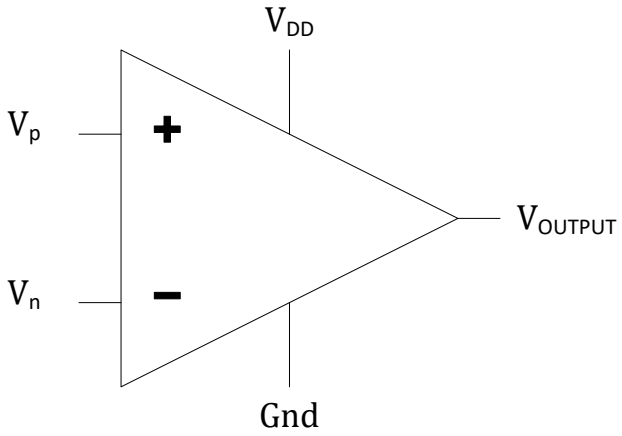

Figure 2.15: Comparator

In figure 2.15 if

$$V_p > V_n \quad then \quad V_{OUTPUT} = Logic\,high \quad or \quad V_{DD} \tag{2.53}$$

else

$$V_n > V_p \quad then \quad V_{OUTPUT} = Logic\,low \quad or \quad Gnd \tag{2.54}$$

For very simple applications a comparator can be made by using an operational amplifier or a differential pair in current mode logic but for more sophisticated designs a practical comparator circuit is needed where sensitivity and propagation delay are very important factors.

A complete block diagram of the comparator is shown in figure 2.16.

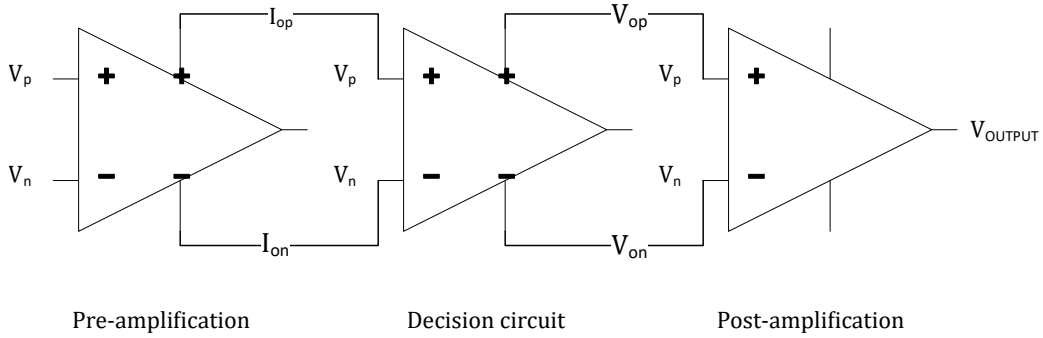

Figure 2.16: Voltage comparator block diagram

A high performance comparator circuit considering sensitivity and propagation

delay consists of three stages mentioned below:

- Pre-amplification stage
- Decision Circuit
- Output buffer or Post-amplification stage

Pre-amplification

The first stage of the comparator consists of a differential amplifier with an active load. By choosing proper dimensions for the M_1 and M_2 the transconductance and the input capacitance of the comparator can be adjusted. Figure 2.17 shows the circuit level implementation. This circuit operates at high speed due to the fact that there is no high impedance node except the input and the output. For small input voltage differences $V_p - V_n$ the output currents can be calculated by using the relationship mentioned below:

$$i_{op} = \frac{g_m}{2}(V_p - V_n) + \frac{I_{ss}}{2} = I_{ss} - i_{on} \tag{2.55}$$

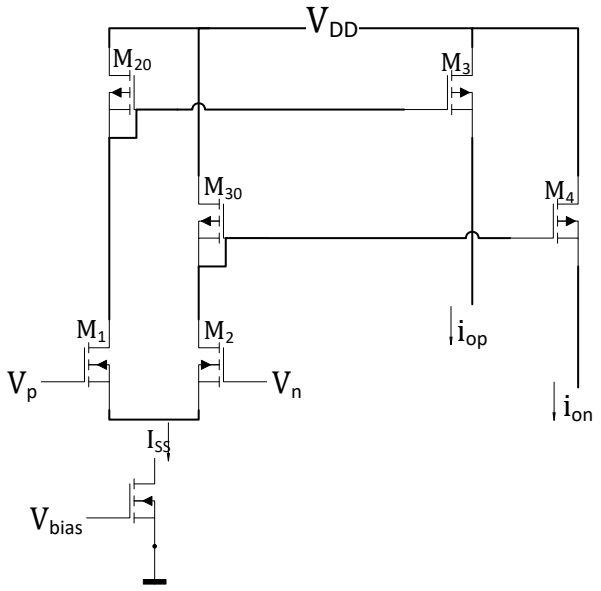

Figure 2.17: Comparator pre-amplification stage

it should be however noted that if $V_p > V_n$ then i_{op} is higher than i_{on}. while if $V_n > V_p$ then i_{on} is higher than i_{op}.

Decision Circuit

The decision circuit is the core of the voltage comparator. Hysteresis can be used here to reject noise in mV level signals. This circuit uses transistors connected in cross topology to increase positive feedback gain. Circuit level implementation is shown in figure 2.18.

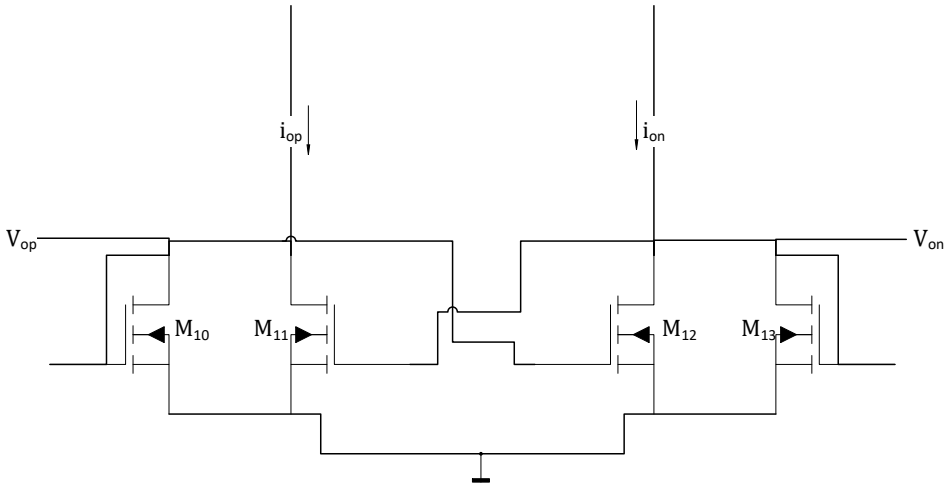

Figure 2.18: Comparator decision stage

To analyse the circuit we suppose i_{op} is much higher than i_{on} in this case transistors M_{10} and M_{12} are in ON state while transistors M_{11} and M_{13} are in the off state. Let suppose $\beta_{10} = \beta_{13} = \beta_A$ and $\beta_{11} = \beta_{12} = \beta_B$ then V_{on} ideally ≈ 0 and V_{op} should be

$$\sqrt{\frac{2i_{op}}{\beta_A}} + V_{THN} \tag{2.56}$$

In figure 2.18 when i_{op} starts decreasing and i_{on} gradually starts increasing there comes a point in time when the gate source voltage of M_{13} becomes larger than V_{TH} at that point current in M_{11} starts increasing which causes a decrease in current from M_{10}. This also causes a decrease in drain source voltage of both M_{10} and M_{11} to decrease which shuts down M_{12}. Just before M_{13} turns on, the current flowing through M_{12} at that point will be

$$i_{on} = \frac{\beta_B}{2}(V_{op} - V_{TH})^2 \tag{2.57}$$

and the current flowing through M_{10} will be

$$i_{op} = \frac{\beta_A}{2}(V_{op} - V_{TH})^2 \tag{2.58}$$

At the switching point current flowing through M_{10} and M_{12} will be equal. which can be written as:

$$i_{op} = \frac{\beta_A}{\beta_B} i_{on} \tag{2.59}$$

If hysteresis is desired in the decision circuit then the currents i_{on} and i_{on} should not be equal at the switching point which requires $\beta_A \neq \beta_B$.

Post-amplification

The last stage of the comparator is the post-amplification or buffer stage. This circuit makes sure that output of the comparator settles to either low which is 0 or high logic signal which is V_{DD}. A differential amplifier shown in the figure 2.19 can be used for the output buffer stage and an inverter can be added afterwards to further increase the gain.

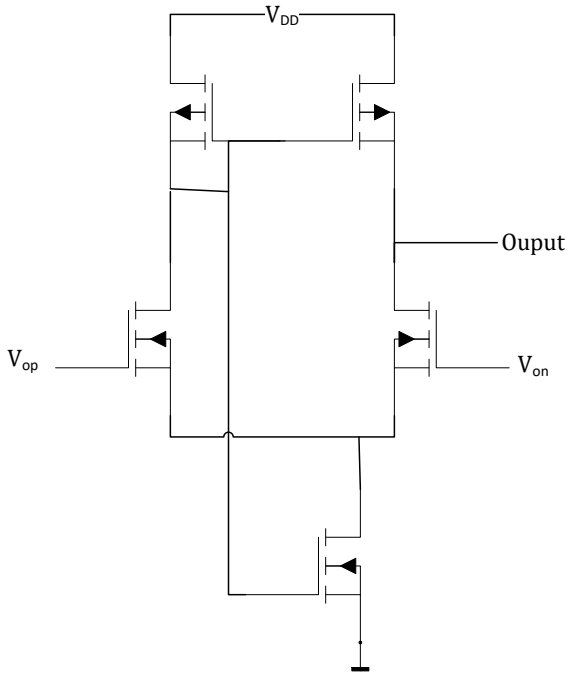

Figure 2.19: Comparator output buffer

Different performance parameters are taken into account to characterise com-

parators which are mentioned below:

- DC Performance
- Transient Response
- Propagation Delay

3 Implementation and Simulation Results

3.1 Regulators

3.1.1 Shunt Regulator

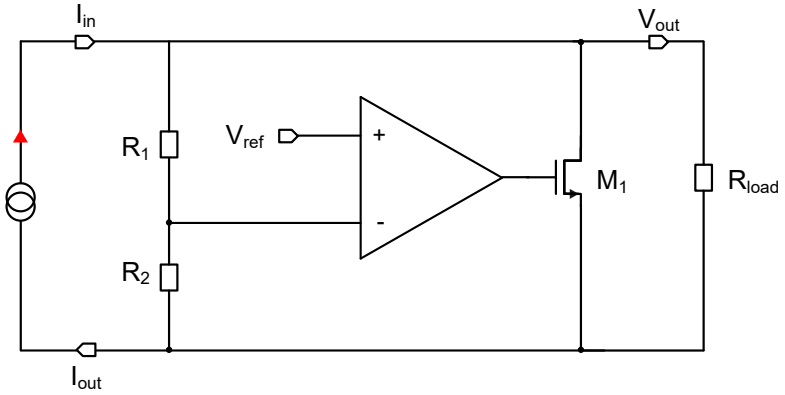

Figure 3.1: Shunt regulator

Figure 3.1 shows the circuit level implementation of a shunt regulator. An input supply current of upto 50mA is applied. R_1 and R_2 implement feedback network and M_1 is the shunt element. This shunt element can be either a PMOS or a NMOS. In this master thesis, the shunt regulator is designed with a PMOS shunt element because of the fact that source is at the regulator output potential and exhibits low output impedance. The error amplifier has its non-inverting input connected to a reference voltage which is provided by a bandgap reference circuit and the inverting input is connected to the resistive feedback network.

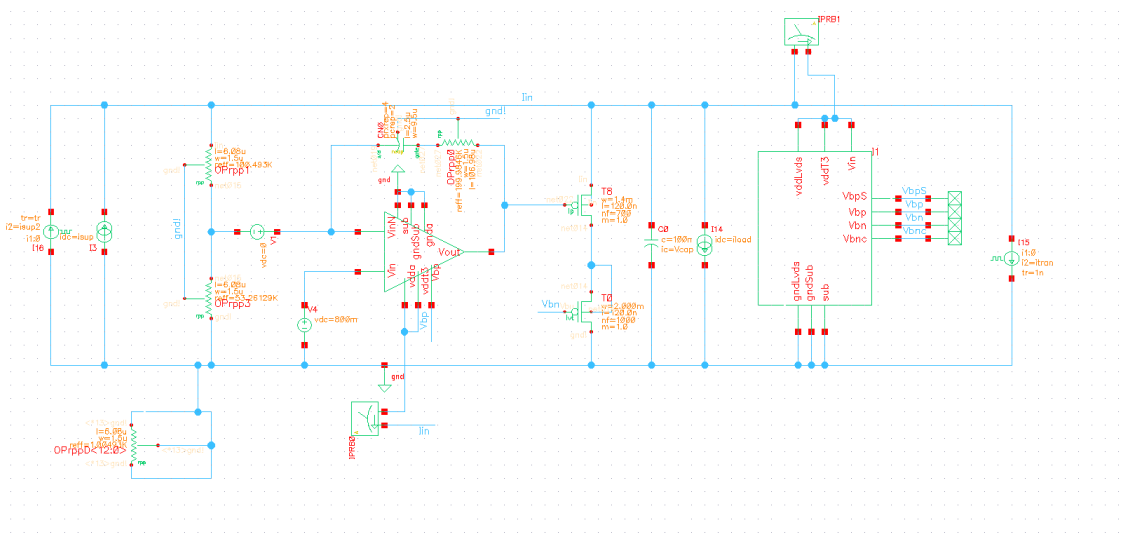

Figure 3.2: Shunt regulator schematic

Figure 3.2 shows the actual schematic of the shunt regulator. The capacitor C_0 is connected in parallel to the load to provide filtration and to provide extra current during the high speed transitions while it takes some time for the error amplifier to adjust the current through the shunt element. T_8 is the actual PMOS shunt element and another transistor T_0 is used to protect the shunt transistor from an over-voltage condition. The protection is necessary since the whole shunt circuitry consists of thing-gate oxide transistors which in the given technology can bear a voltage of up to 1.6V while the generated shunt regulator output voltage is 2.3V. Miller compensation is added in the negative feedback for error amplifier to introduce a pole and zero for better stabilization by increasing the phase margin. If the output voltage drops from the regulated value of $2.3V$ then initially the capacitor is discharged. As a result the voltage across the resistor $OPrpp3$ decreases so it causes the inverting input of the amplifier to be lower than the non inverting input so the output of amplifier increases which causes a decrease in the value of current passing through the PMOS shunt element. This causes an increase in current flowing to the load to stabilize the output voltage. On the other hand if the output voltage increases this causes an increase at the inverting input of the amplifier. When the inverting input is more than the non inverting input the output voltage of the amplifier decreases. A voltage decrease at the gate of the PMOS shunt element causes an increase in the current passing through it. This operation brings down the output to the regulated value.

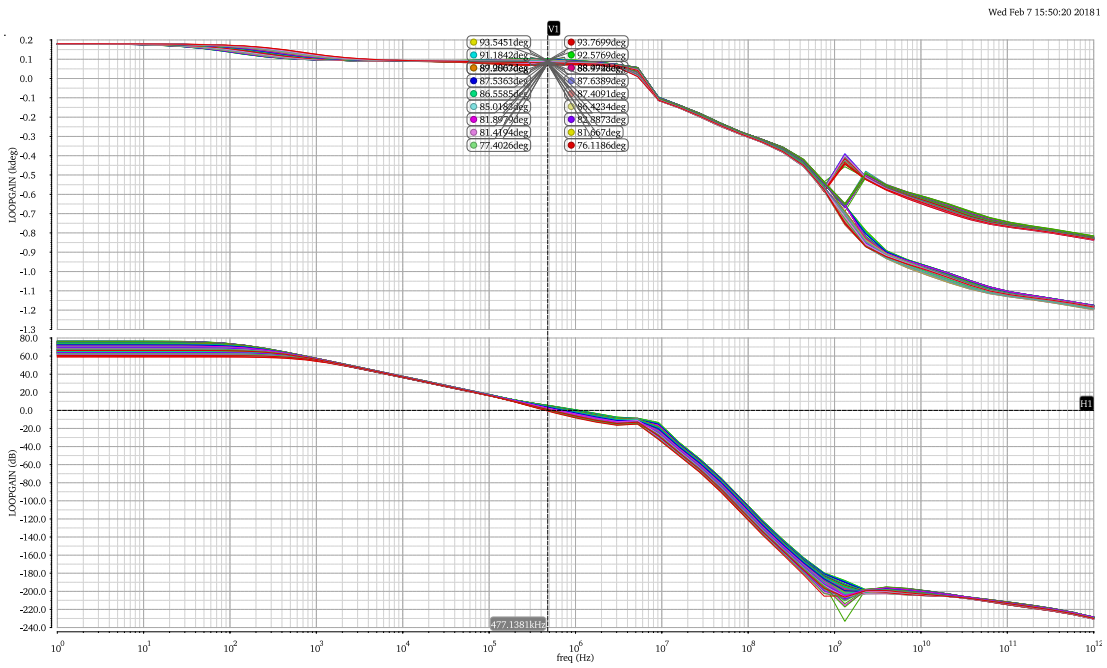

Figure 3.3: Shunt regulator phase/gain margin

The shunt regulator circuit is simulated using the virtuoso design environment from cadence design systems for the corners $ff, fff, fs, sf, ss, ssf, tt$ and the operating temperatures of $-50°$,27° and 60° Celsius. Additionally, a load current variation of 0 to 45mA is also considered. Figure 3.3 shows the open-loop gain of the designed shunt regulator. The position of the voltage source V1 indicates the point where the regulation loop has been broken. Phase and gain margins are quantities which show how the system will behave. A positive gain and phase margin indicate that there is still some safety margin before the system is going unstable. Gain margin is derived from the open loop gain plot at the point in the bode plot where the phase reaches -180 degrees. If a straight vertical line is drawn at this point then the crossing of the vertical line with the magnitude curve corresponds to the gain margin. This is the amount of additional gain which would lead the system to become unstable. Similarly, phase margin can be extracted from the Bode open loop plot at the point where the gain is 0dB. Which means that the gain is unity and as a result the input and the output have the same magnitude. So, if a verticle line is drawn at 0dB then the difference between -180 degrees and the crossing point of the vertical line with the phase plot in the open-loop Bode plot corresponds to phase margin. Simulations show for all corners and temperatures a minimum gain margin of 10dB and a phase

margin $> 60°$.

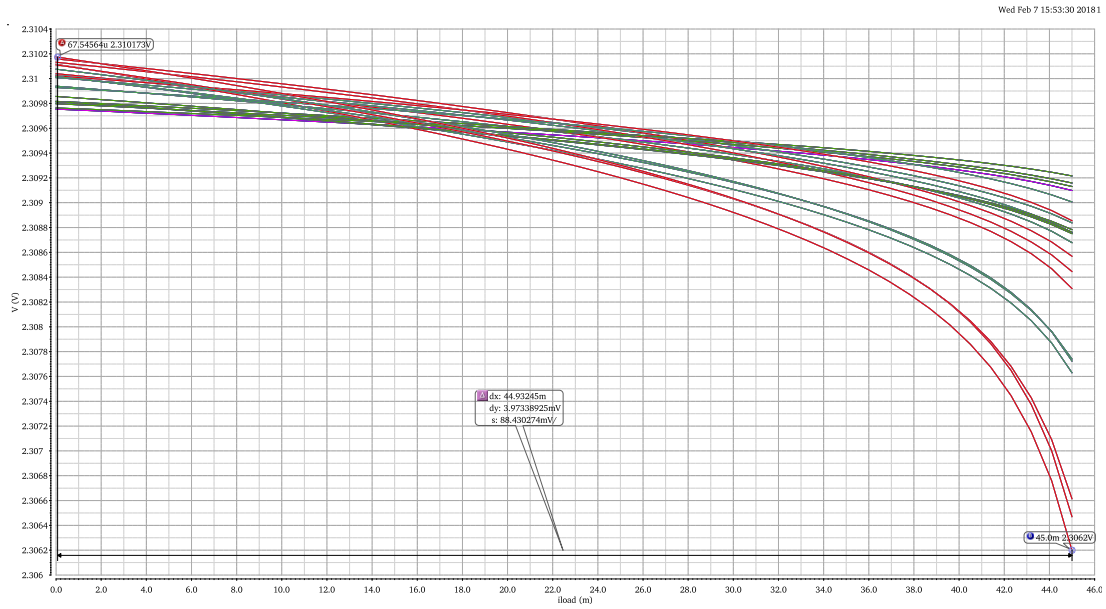

Figure 3.4: Shunt regulator load regulation

Figure 3.4 shows the load regulation behaviour for the shunt regulator. When the load is increased from 0 to 45mA (maximum load), the maximum deviation is 4mV around 2.3V for all corners and temperatures.

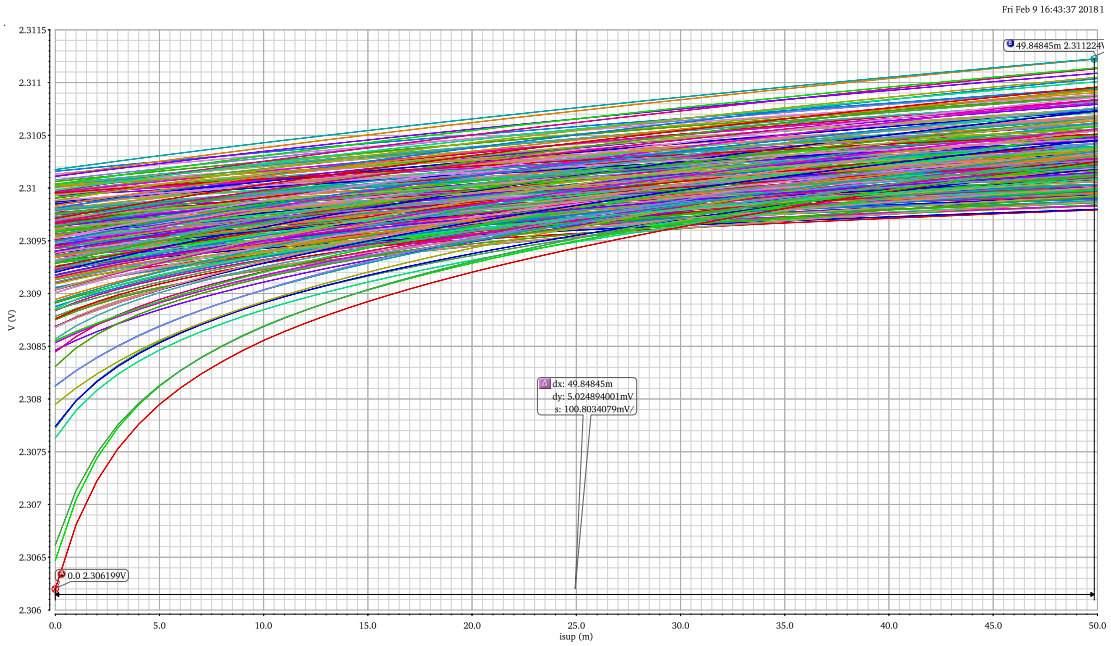

Figure 3.5: Shunt regulator line regulation

Figure 3.5 shows the line regulation characteristic of the shunt regulator. As can be seen from the graph a change of input supply current from 0 to 50mA causes a deviation of 5mV in the worst case.

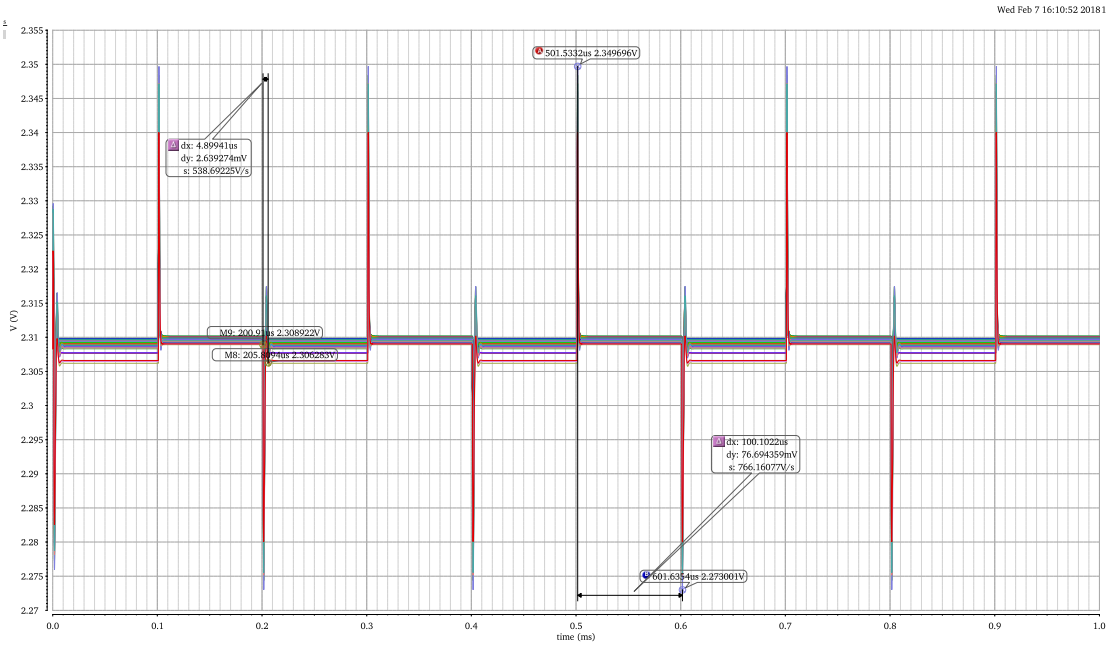

Figure 3.6: Shunt regulator transient simulation

Peaking behaviour seen in the figure 3.6 is due to the fact that the load is transient and it changes abruptly. A transient load of 15mA is used with a rise time of 1ns because of this abrupt change the error amplifier needs some time to adapt to the new load conditions and to regulate the output voltage. The maximum difference from one peak to the other is around 76mV while the duration of each peak is very short and 4.8μs.

3.1.2 Linear Regulator

As mentioned earlier a pass element in the linear regulator can be a PMOS or NMOS. Any of these pass devices have their own advantages and drawbacks, some of them are mentioned in the previous chapter. In the designed circuit shown in figure 2.4 a NMOS pass device is used which results in a simpler compensation scheme and does not require an external capacitor but comes at price of higher dropout voltage as compared to PMOS transistors. Another advantage of the NMOS pass element is that the output impedance will be very small due to the source connected to the output.

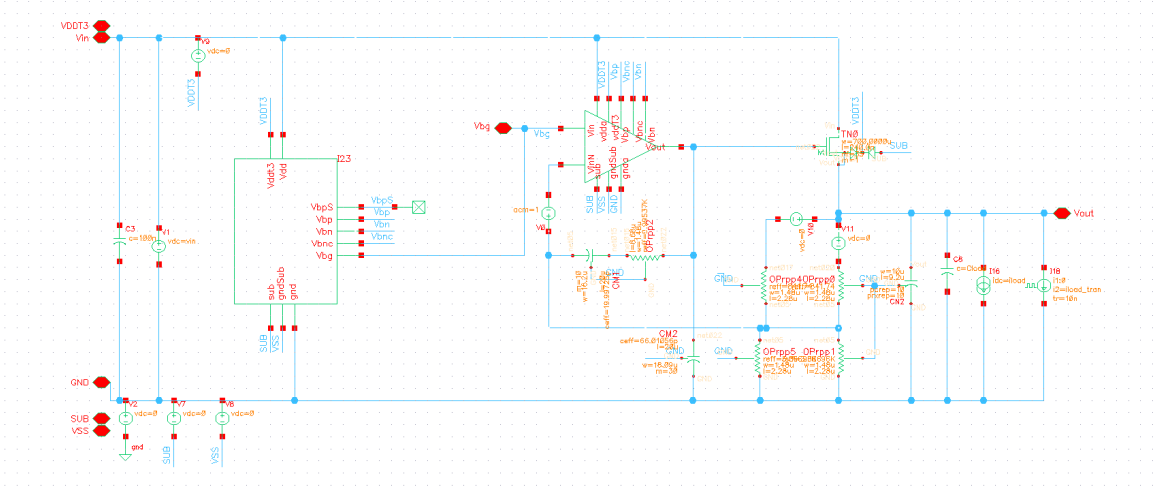

Figure 3.7: Linear regulator schematic

Figure 3.7 shows the actual implementation of the Linear regulator. TN0 is the NMOS pass device. The input of this regulator is connected to the output voltage of the shunt regulator designed earlier which is 2.3V. When the load current at the output of the Linear regulator is increased a decrease in output voltage is caused. This decreased output voltage is sensed through the feedback network which is connected to the inverting input of the error amplifier. When the inverting input is smaller than the non inverting input the output voltage of the amplifier goes high which causes an increase in the current going through the pass device. In the other way if the output voltage goes high the inverting input of the amplifier is larger than the non inverting input so that the amplifier output voltage decreases which also decreases the current passing through pass device to lower the output voltage.

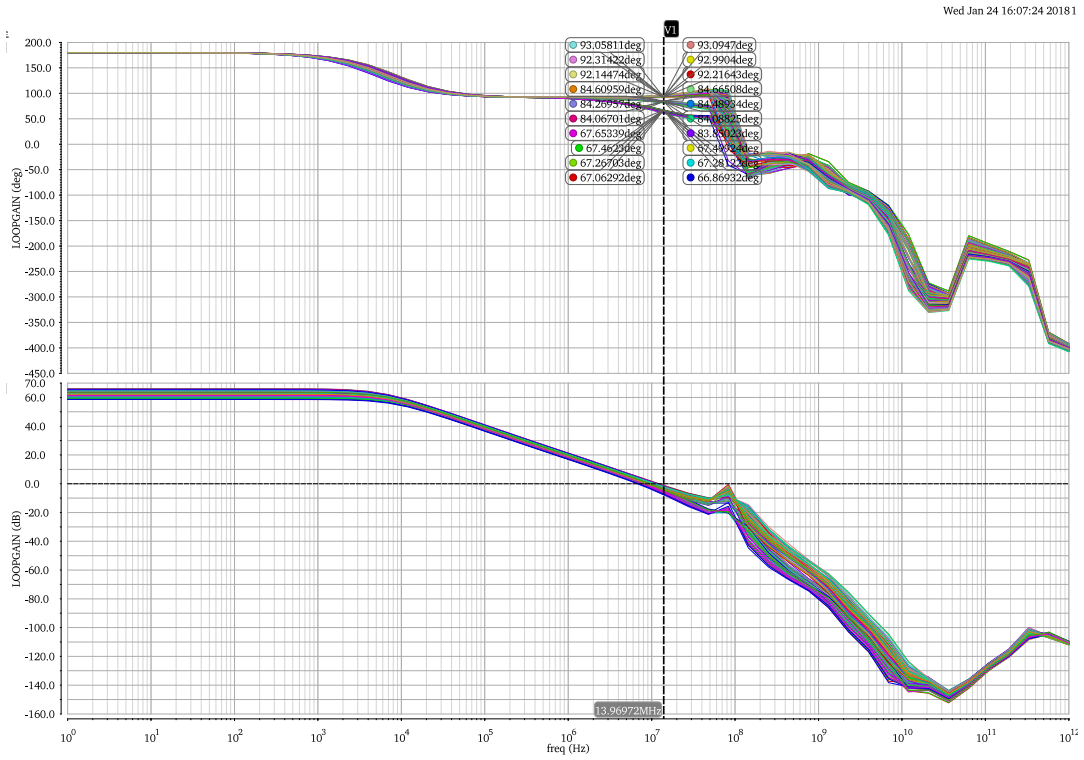

Figure 3.8: Linear regulator phase/gain margin

Definition of gain and phase margin are the same as defined in the description of figure 3.3. Here in this graph, we can see that the minimum phase margin is around 66 degrees which is sufficient to ensure stability. Similarly, the gain margin can be found by placing a vertical marker at the point where the phase shift is -180 degree and then looking at the value of gain in dBs. In case of the Linear regulator, the minimum gain margin for all the corners is higher than 10dB. The corners for the linear regulator are same as defined in the description of the figure 3.3.

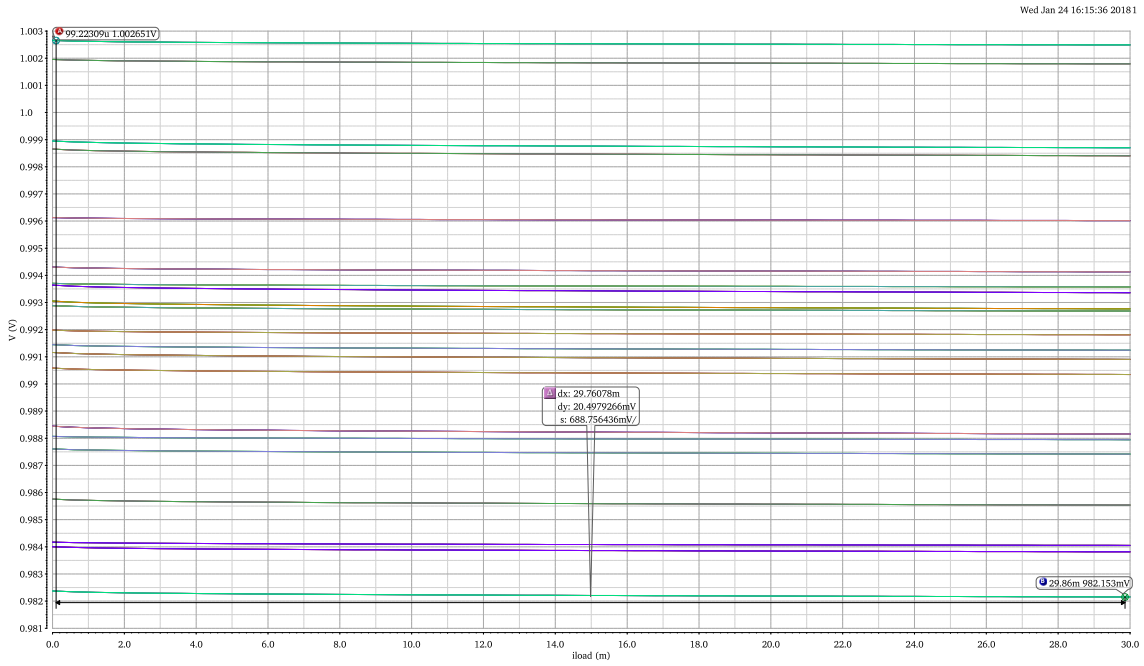

Figure 3.9: Linear regulator load regulation

This Linear regulator is designed to have an output of 1.0V. Figure 3.9 shows the load regulation. The load is varied from 0 to 30mA and the maximum deviation is around 20mV in the worst case.

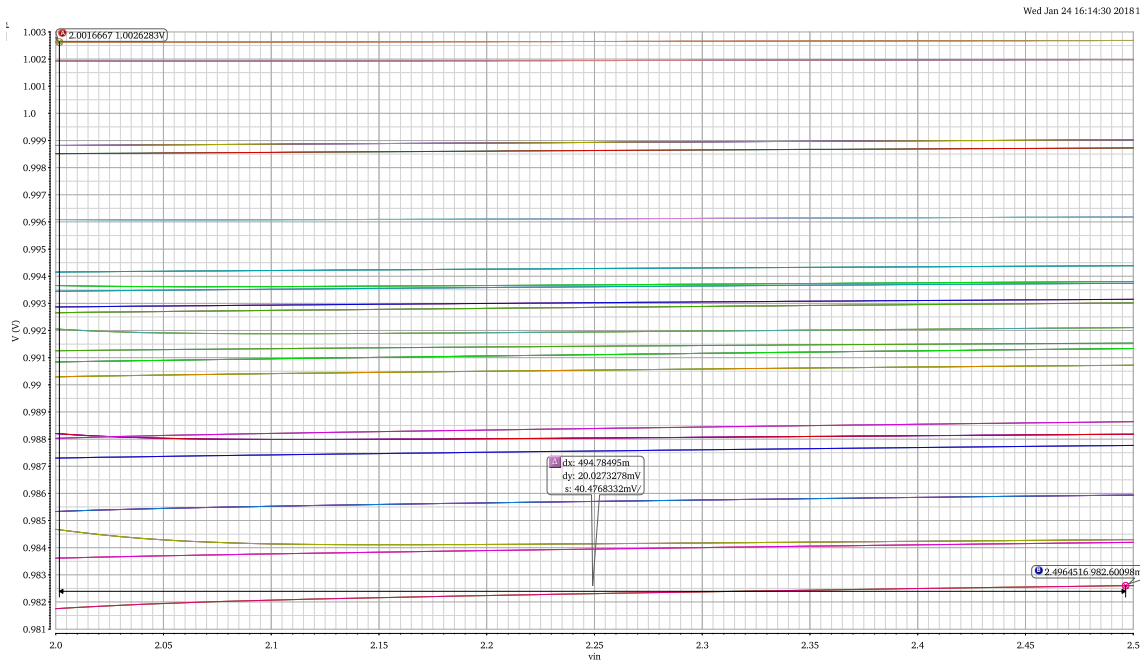

Figure 3.10: Linear regulator line regulation

For the line regulation the input is varied from 2.0V to 2.5V. As it can be seen in the figure 3.10 the maximum variation in the regulated output voltage is around 20mV.

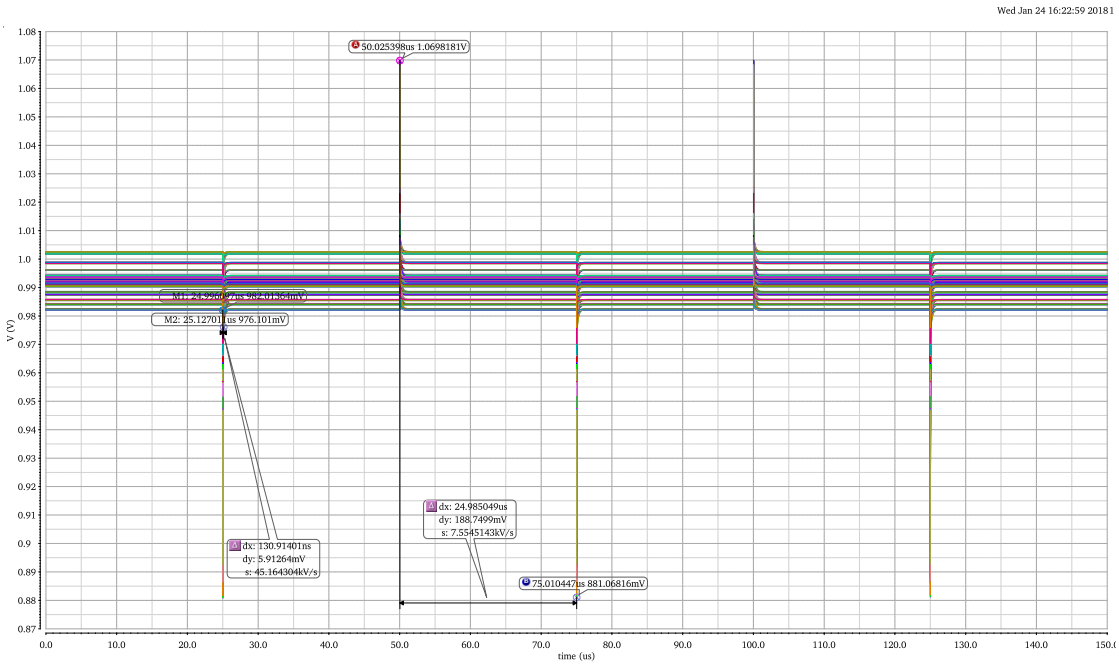

Figure 3.11: Linear regulator transient simulation

Figure 3.11 shows the transient simulation. Peaking behaviour is due to abrupt change of load condition. When the load is increased the output voltage drops however the error amplifier needs time to react to this voltage which causes negative peaking. Positive peak arises when the load is decreased abruptly then output voltage reaches very high levels for a small period of time until the error amplifier reacts. The time duration for this peak is very short 130.9ns while the difference between two peaks is around 188mV.

3.2 Power-on-Reset Circuit

As described in chapter 2 section 2.2 the implemented POR circuit use the bandgap reference circuit proposed in [1] which is shown in figure 2.13 as a starting point. To reach the actual POR the feedback path is cut-off, the monitored supply voltage is connected to the passive resistor/diode network which generated V_{ref} voltage of the original bandgap circuit and the operational amplifier is replaced with a comparator. If the supply voltage is switched-on and ramps up the switching point of

the comparator is reached at some point then we see that the point at which both PTC and NTC voltages are equal the comparator goes from logic *low* to *high* or *high* to *low* depending on the polarity. This switching point corresponds to the voltage V_{ref} which is generated with active feedback in the original bandgap circuit where circuit conditions are such that the PTC and NTC voltages are equal.

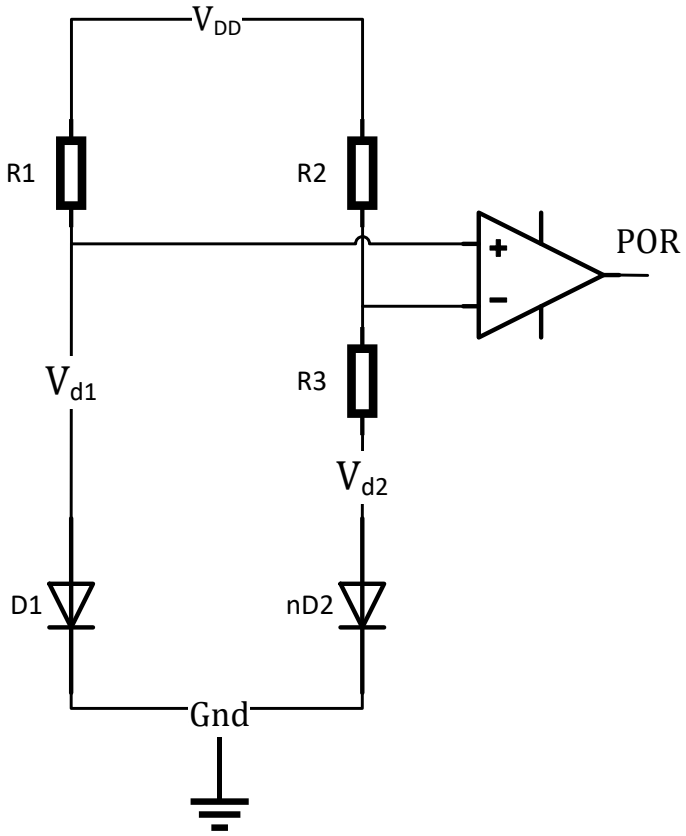

Figure 3.12: Power on reset circuit [2]

The design as it is documented in the literature is based on diodes. This diode based scheme has also been used for initial simulations to verify the circuit operation. However diodes have been proven to be susceptible to radiation [16]. The diode voltage level changes as a function of total ionizing dose. While in a bandgap reference this would give rise to variation in a reference voltage. With radiation dose in the POR circuit, the accumulated radiation would affect the voltage level at which the reset signal is released. Since thing gate-oxide MOS transistors are radiation hard an alternative POR circuit scheme based on MOSFETs has been developed. MOS transistors operated in weak inversion mode behave just like diodes and can be replaced by forward biased diode model mentioned in equation

2.33. MOS transistors provide much better radiation performance but they have the disadvantage of greater process variation.
Depending on the value of the saturation voltage V_{dsat} a MOS transistor can be in one of the following three states.

- $< 75mV$ (weak inversion)
- $> 75mV and < 100mV$ (moderate inversion)
- $> 100mV$ (strong inversion)

Another requirement is to bring this POR output voltage down to 950mV instead of the initial bandgap voltage of 1.25V

3.2.1 Diode Implementation

The POR is shown in figure 3.12. As from equation 2.51 for a zero temperature coefficient the value of resistors R_2 and R_3 must be chosen in such a way that

$$(1 + \frac{R_2}{R_3}) \ln n \approx 17.2 \tag{3.1}$$

Simulation results for diode based bandgap and POR are shown in the next few pages.

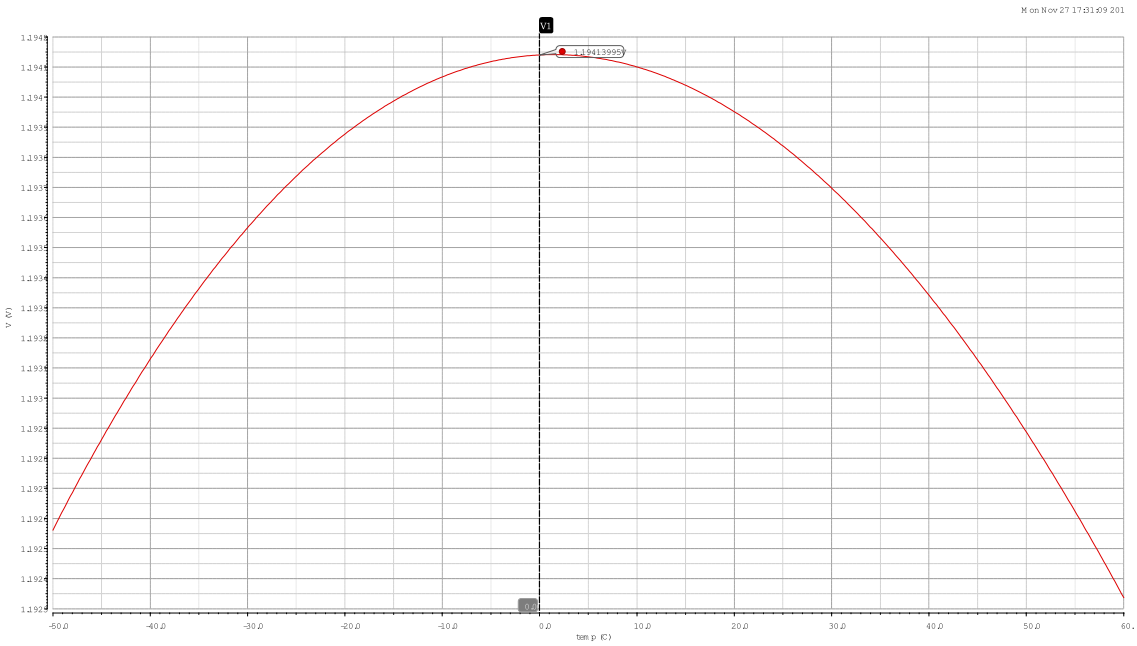

Figure 3.13: Bandgap Simulation with Diode

Figure 3.13 shows the reference voltage from bandgap circuit. Around $1.2V$ it shows zero temperature coefficient.

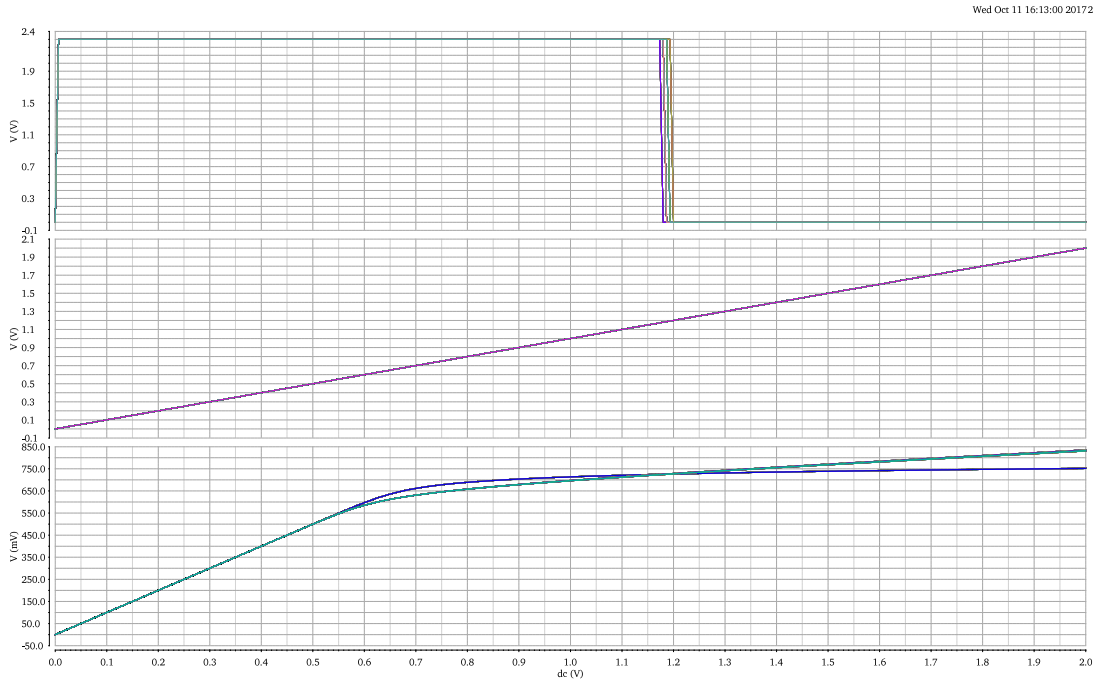

Figure 3.14: POR DC simulation using diode

As can be seen from 3.14 that the crossing point is such that circuit releases the reset around $1.2V$ but our requirement is that it should be around $950mV$.

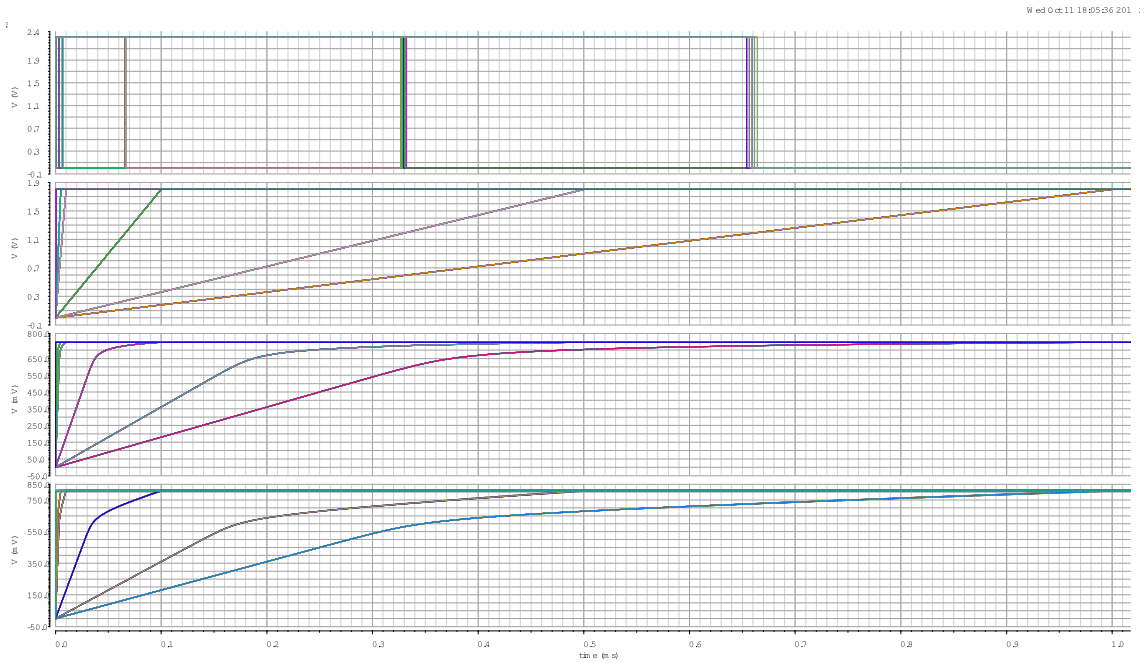

Figure 3.15: POR transient simulation using diode

Figure 3.15 shows the transient simulation for different rise times. The rise times chosen for the transient simulation are 100n, 1μ, $5\mu, 10\mu, 100\mu, 500\mu$ and $1m$. The POR circuit worked for all of these rise times.

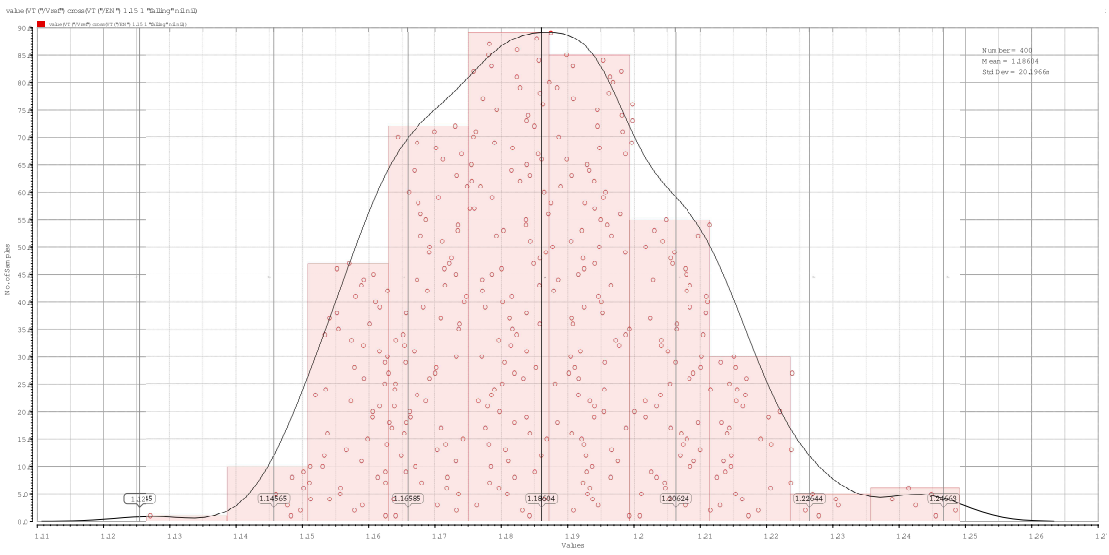

Figure 3.16: POR Monte Carlo simulation using diode

Figure 3.16 shows Monte Carlo simulation for POR using diodes in which a

standard deviation of 20.19mV is observed. As a result, the switching point of the POR signal will vary around ± 60.6 mV.

3.2.2 MOS Implementation

As mentioned earlier a MOS transistor behaves just like a diode if operated in weak inversion condition i.e. $V_{dsat} < 75mV$.
Four different implementation variants were implemented using MOS transistors to compare which one suits better to our requirements. There are mainly two type of transistors, core and IO transistors. Core transistors are used in the core of circuitry IC, they have small threshold voltages and thin gate oxide. As a result they are radiation hard. IO transistors on the other hand have large threshold voltages and thick gate oxide and are not radiation hard.
Core transistors are further divided into few categories of which two are mentioned here. LP (Low power transistors) and normal ones. Low power transistors have larger threshold voltages compared to the normal transistors V_t.

POR with MOSFET

When using normal core MOS transistors, temperature stability of the switching point is reached for resistor $R_1 = R_2 = 10k$ while $R_3 = 2.5k$. V_{ref} is around 486mV which is too low. Therefore different topologies are simulated to get the switching point at a voltage around 950mV.

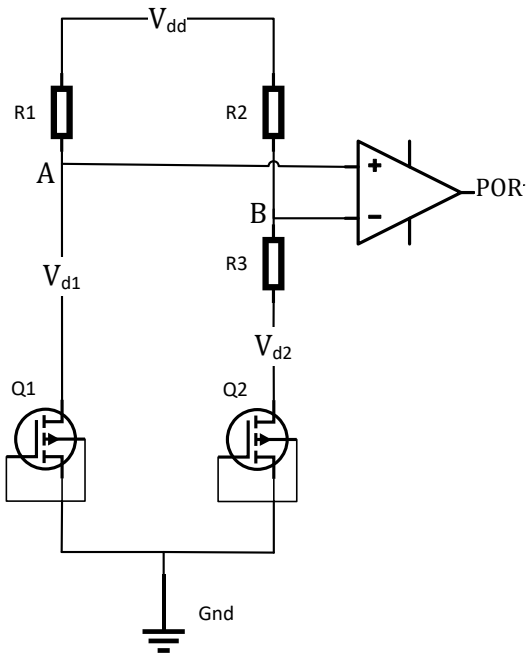

Figure 3.17: POR using DTMOS transistors

In figure 3.17 the POR circuit based on MOS transistors is shown. In this circuit the diodes have been replaced by PMOS transistors which have a connection between their gate and drain terminals. In addition the bulk terminal of both transistors is shorted to drain instead of source. Normally bulk terminal of MOSFETs should be connected to the lowest potential in case of NMOS and to the highest potential in case of PMOS. So, for both cases bulk terminal should be connected to source terminal. This is to make sure that junction diodes are reverse biased and there are no leakage currents. For this POR circuit we are using the technique DTMOS (Dynamic Threshold MOSFET) in which the junction diodes are forward biased for better matching. As is described in detail in [13] the matching of two DTMOSFET's is twice as good as normal source bulk connected devices. Using dynamic threshold MOSFET lowers the power consumption and they are more process tolerant for bandgap reference circuits [13].

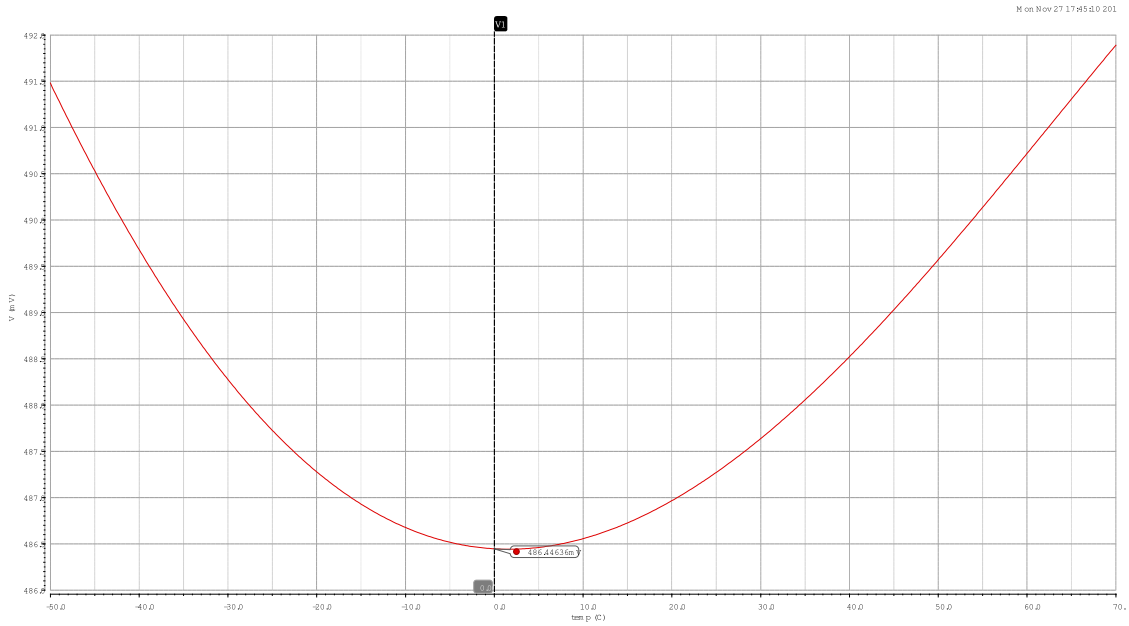

Figure 3.18: POR bandgap simulation using MOS

Replacing the diodes in the bandgap circuit by MOSFETs in diode configuration reduced the bandgap reference voltage to 486mV while a deviation of around 5mV is observed going from temperature -50 to 60 degrees as is shown in figure 3.18.

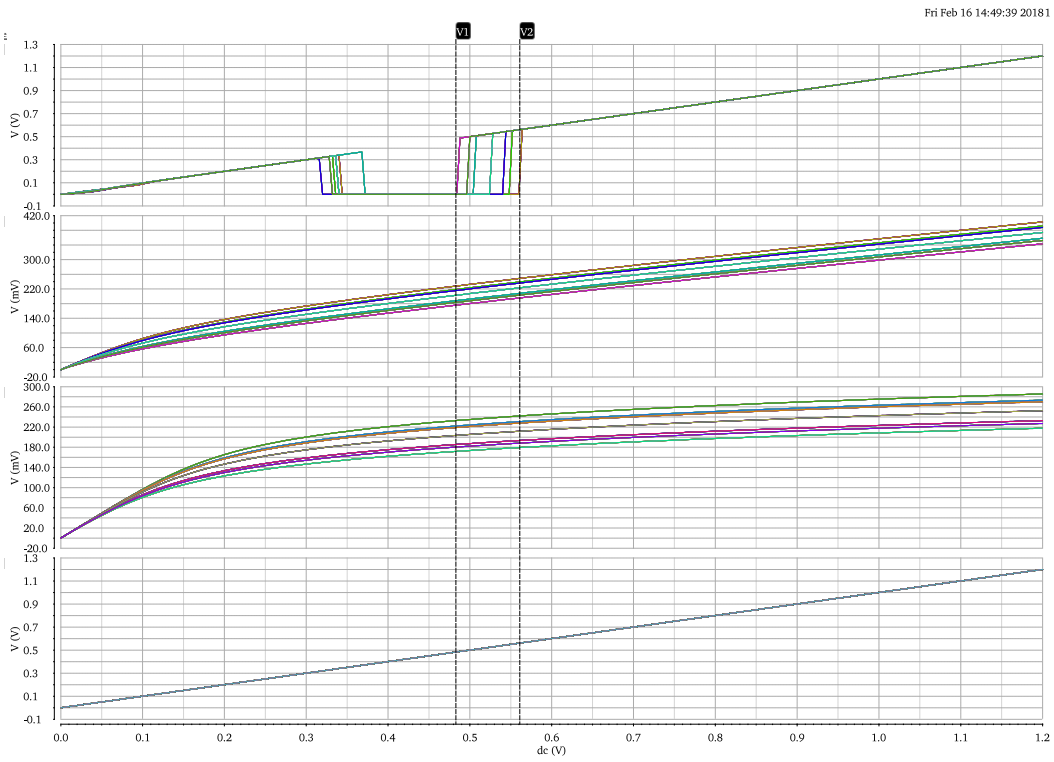

Figure 3.19: POR DC simulation using MOS

Looking at the figure 3.19 the top most graph shows the output reset signal. The second and the third graph shows NTC, PTC voltages at nodes A and B respectively in circuit given in the figure 3.17. The POR circuit is simulated using the virtuoso design environment from cadence design systems for the corners $ff, fff, fs, sf, ss, ssf, tt$ and the operating temperatures of $-50°$,$27°$ and $60°$ Celsius. The last graph plots input power supply voltage V_{dd}. We can see that when simulated for all corners and temperatures the output reset voltage varies from 0.48V to 0.56V. As the power of comparator is tied to the same power source of bandgap core, it can be seen that the output reset voltage follows the input until around 350mV and then applies the reset signal. The reset signal is applied until 480mV for the corner with the minimum value.

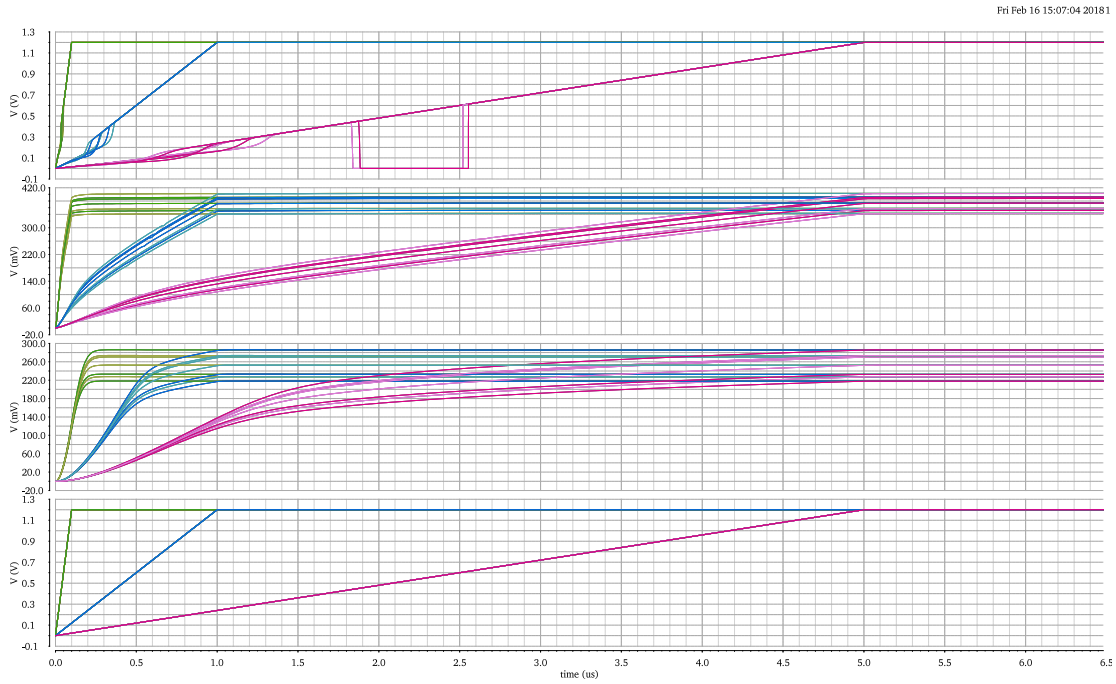

Figure 3.20: POR fast transient simulation using MOS

Figure 3.20 shows fast transient simulation. The rise times chosen for fast transient simulation are 100n,1μ and 5μ. For these rise times the circuit does not work except for few corners. As explained in the last diagram, the top most graph shows the output reset signal and it can be seen that output just follows the input. After 350mV it should apply a low signal of 0V. Both PTC and NTC voltage have no crossing point except for few corners.

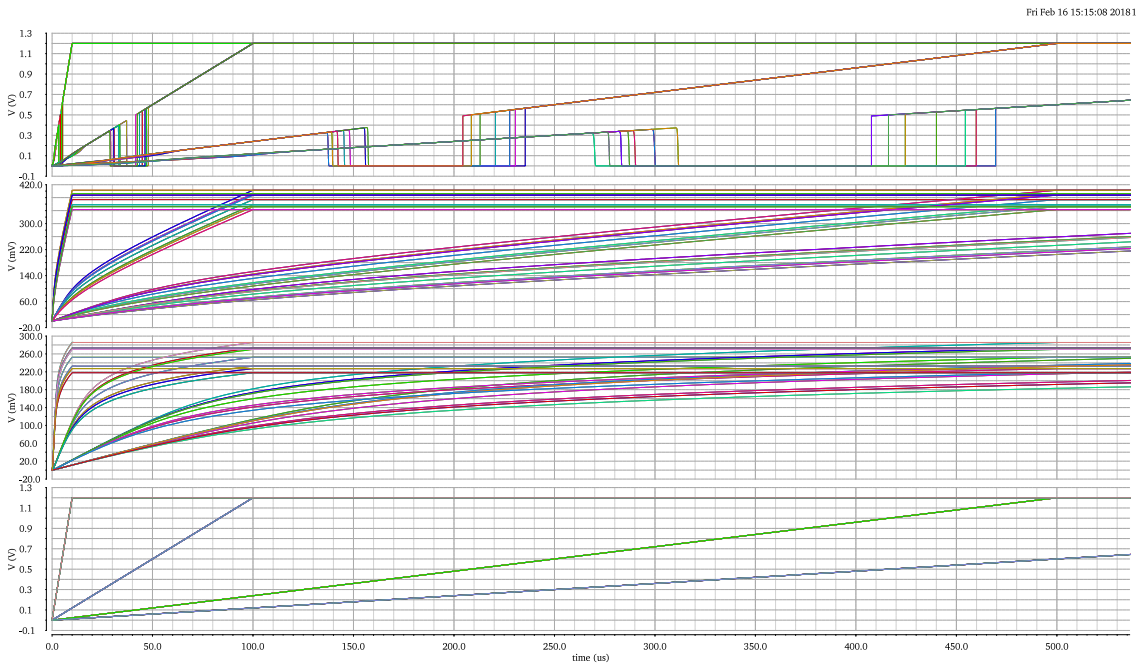

Figure 3.21: POR slow transient simulation using MOS

In the previous diagram 3.20 it can be seen that for fast transient times circuit did not work properly however it works for transient rise times more than 10μ. Figure 3.21 shows the simulation for rise times of $10\mu, 100\mu, 500\mu$ and $1m$. For rise time more than 10μ the circuit works properly for all corner and temperatures.

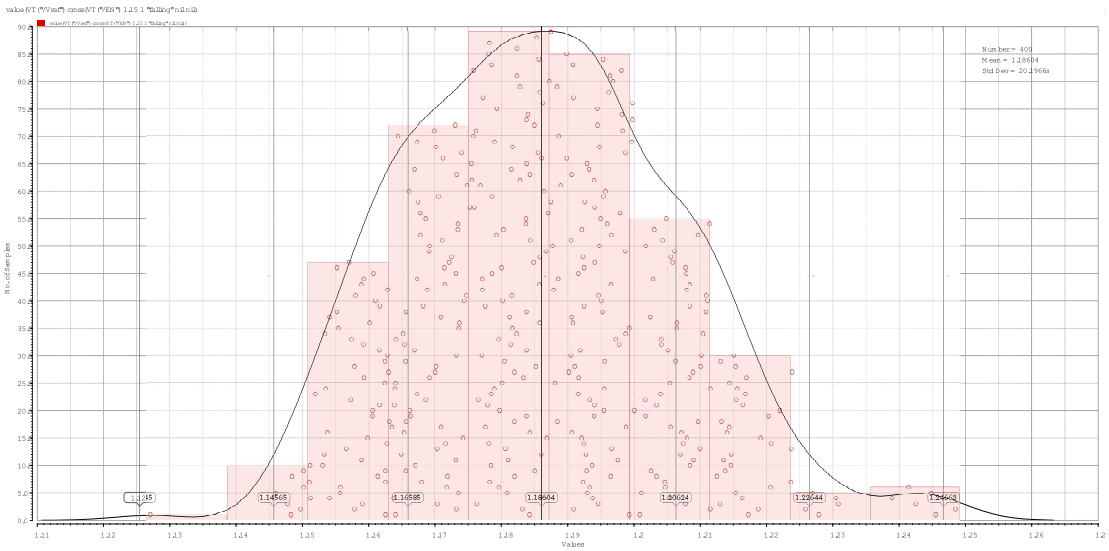

Figure 3.22: POR Monte Carlo simulation using MOS

As shown in figure 3.22 Monte Carlo simulations of the POR circuit using MOS

transistors result in a standard deviation of 20.19mV. As a result, the switching point of the POR signal will vary around ± 60.6 mV.

Low power MOSFET

Using low power MOS transistors, temperature stability of the switching point is reached for resistors $R_1 = R_2 = 14k$ while $R_3 = 2.2k$. V_{ref} is around 840mV. The output voltage swing can be increased by decreasing the value of the resistances however the MOS transistors leave the weak inversion operation region in this case. Simulation results are not included as this topology is not considered due to low output voltage.V_{dsat} is 68mV.

Normal MOSFETs in series

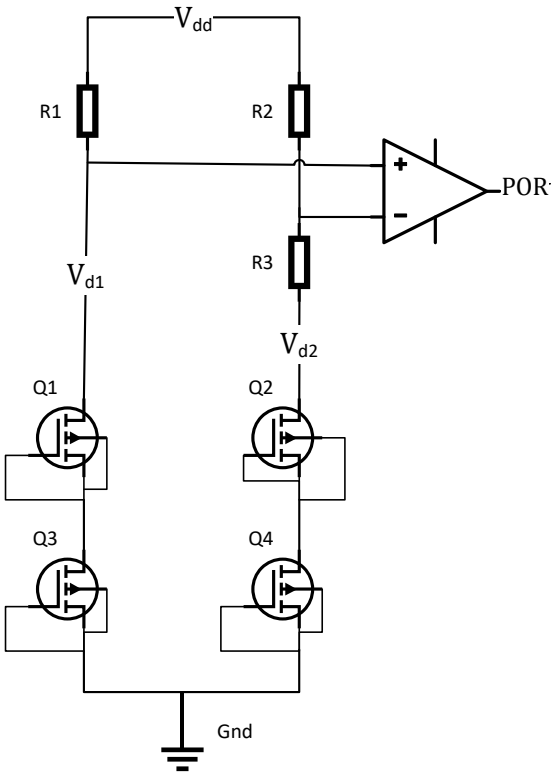

Figure 3.23: POR using two MOSFETs in series

The circuit in figure 3.23 shows the circuit level implementation with two MOS transistors in series. This topology is implemented to increase the switching point voltage level however an increase in process variations can be observed. Using

this technique resistors values of $R_1 = R_2 = 11.5k$ while $R_3 = 3.3k$ the switching voltage level is around 960mV which is 130mV more than using low power single transistors at same $V_{dsat} \approx 69mV$

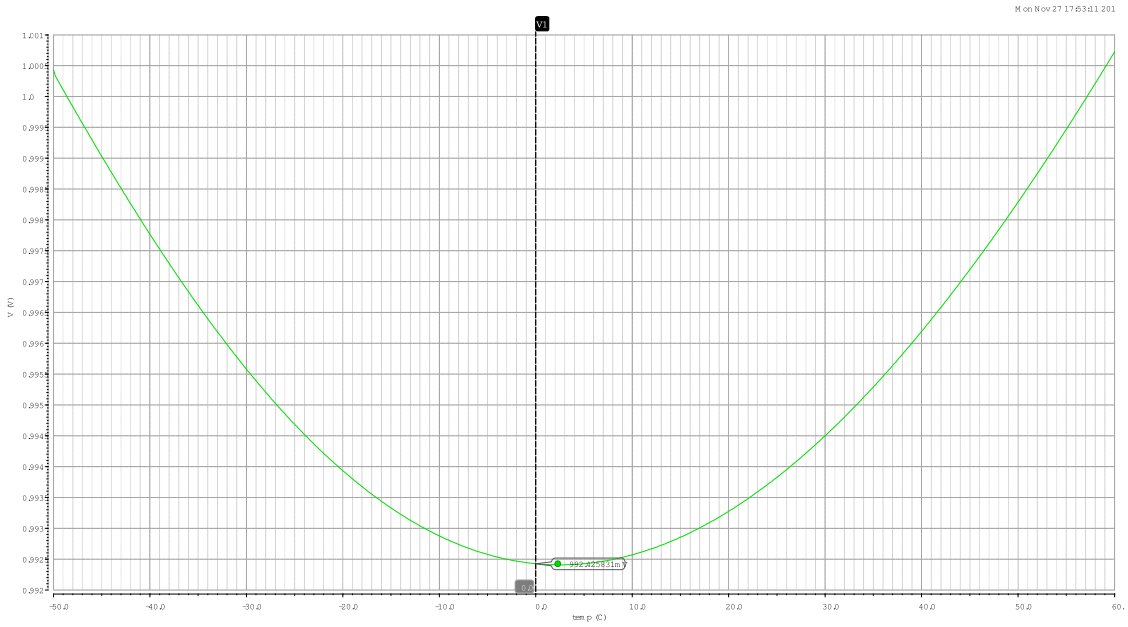

Figure 3.24: Bandgap simulation using MOS in series

The bandgap reference circuit simulation in figure 3.24 shows that by using two transistors in series a V_{ref} of 992mV is generated with zero temperature coefficient around 0° and a maximum variation of 8mV for all temperature and corners.

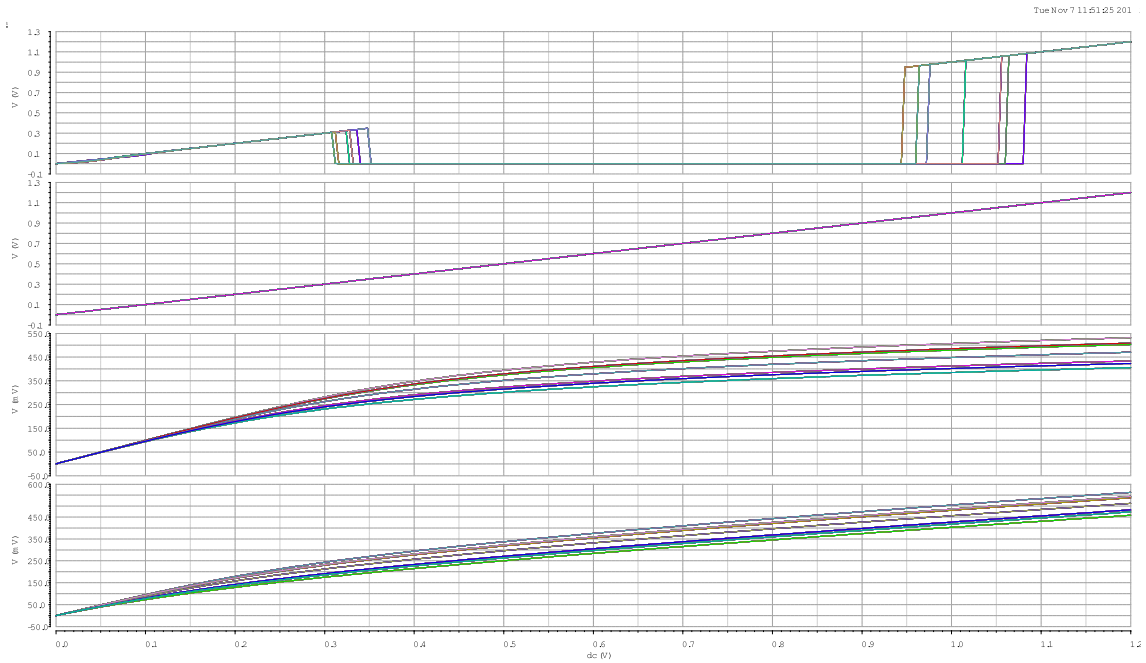

Figure 3.25: POR DC simulation using two MOSFETs in series

Figure 3.25 shows the DC simulation. When simulated for all corners and temperatures it can be seen that the minimum and maximum value until reset is released is around 940mV to 1.06V.

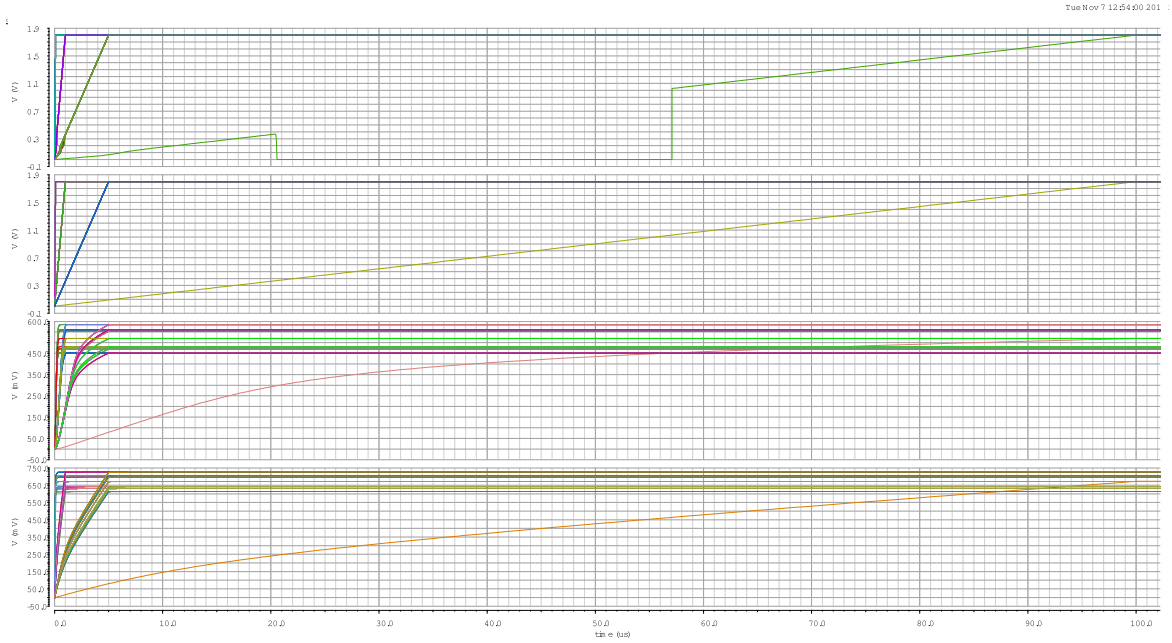

Figure 3.26: POR fast transient simulation using two MOSFETs in series with comparator filter

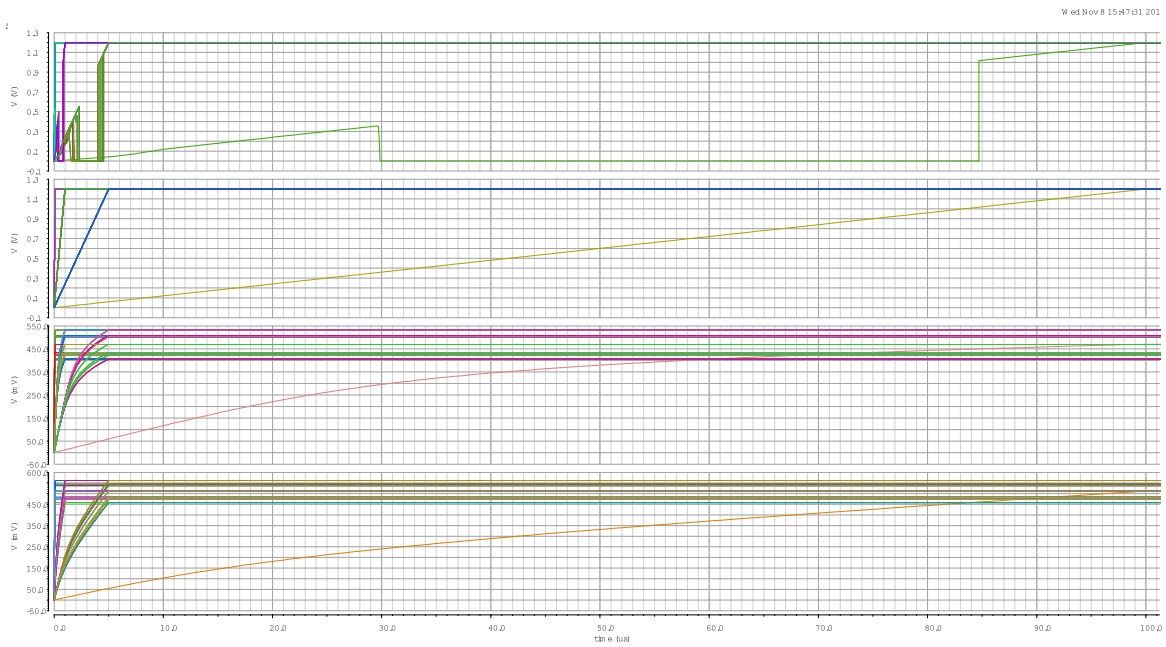

Figure 3.27: POR fast transient simulation using two MOSFETs in series

Figure 3.26 and 3.27 show transient simulation with a low-pass filter at V_n of the comparator inputs [2.16]. Comparator circuit was designed by Mr.Niklaus Lehmann for the DCS chip in [16]. This filter was added to reject noise which would lead to oscillation in the comparator switching point. For the same reason hysteresis was also taken into account for the comparator circuit. Comparing both figures it can be seen that by using the low pass filter at the input, performance is further degraded for faster rise times. Especially there is no crossing point for PTC and NTC voltages for rise-times less than 5μ which causes the output reset voltage to just follow the input voltage, Instead of applying a reset.

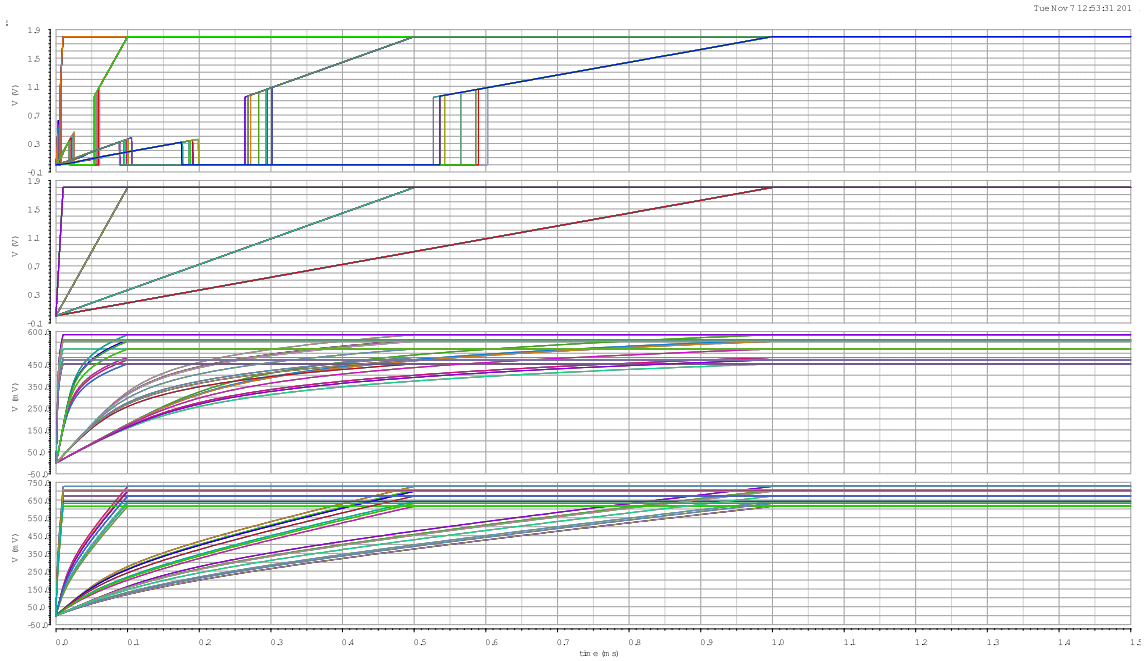

Figure 3.28: POR slow transient simulation using two MOSFETs in series with comparator filter

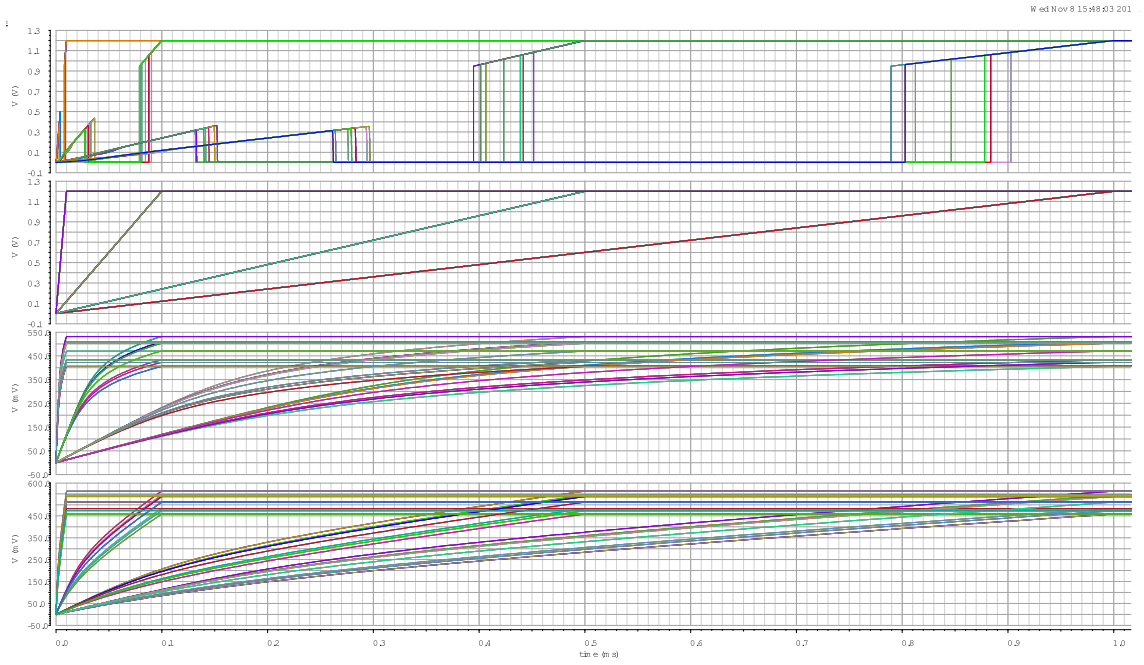

Figure 3.29: POR slow transient simulation using two MOSFETs in series

Figure 3.28 and 3.29 shows the slow rise times. Even though the circuit works for both conditions i.e. with and without low-pass filter at the comparator input,

the circuit behaves very slow when the filter is applied. The Comparator without filter reacts at-least 300μs faster.

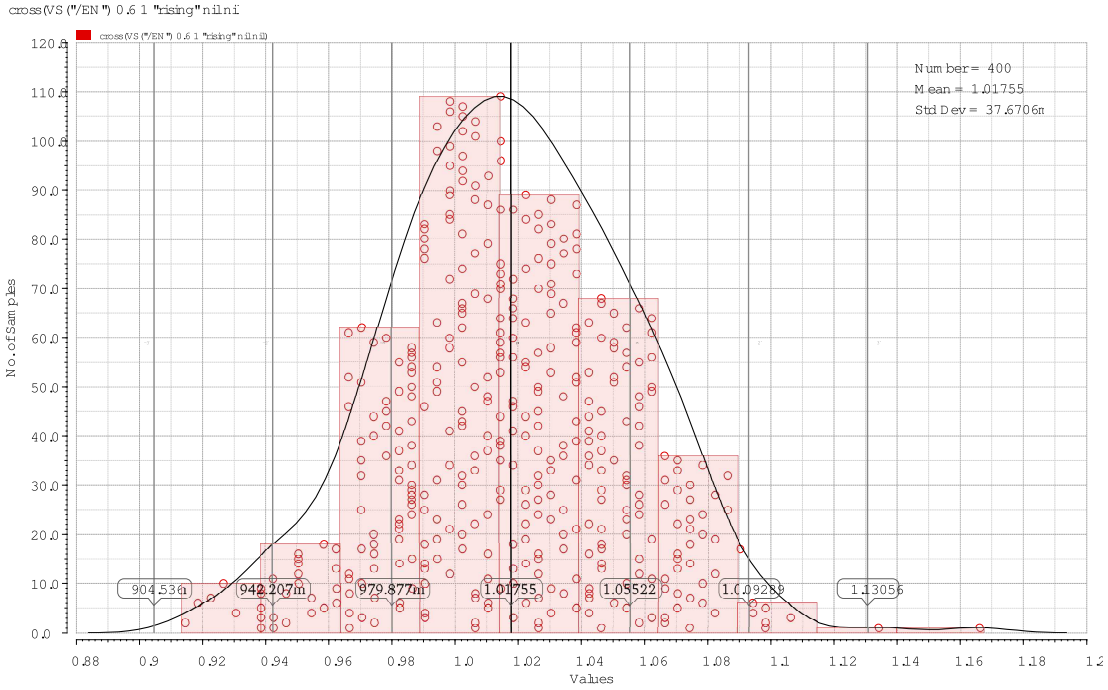

Figure 3.30: POR Monte Carlo simulation using two MOSFETs in series with comparator filter

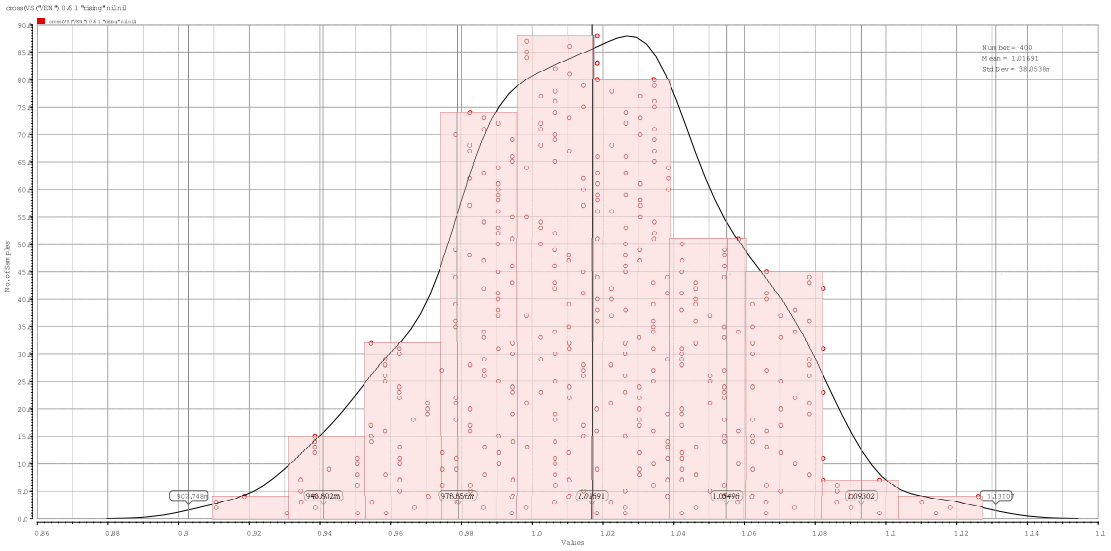

Figure 3.31: POR Monte Carlo simulation using two MOSFETs in series

Low power MOSFETs in series

Using low power transistors in a series configuration and resistor values of $R_1 = R_2 = 80k$ and $R_3 = 16k$ a temperature stable switching point at 1.28 which is much more than our requirement. For the above calculated values V_{dsat} for each transistor is at a maximum of $53mV$ which ensure transistor operation in weak inversion.

3.2.3 Comparator

For the comparator circuit implementation, a noise simulation of the core POR has been performed. Noise simulation has been done for the worst corner and the RMS noise voltage was about 2.07mV. So, for the comparator to work properly hysteresis should be 3 times the noise value for the worst case in order to make sure that there are no oscillations.

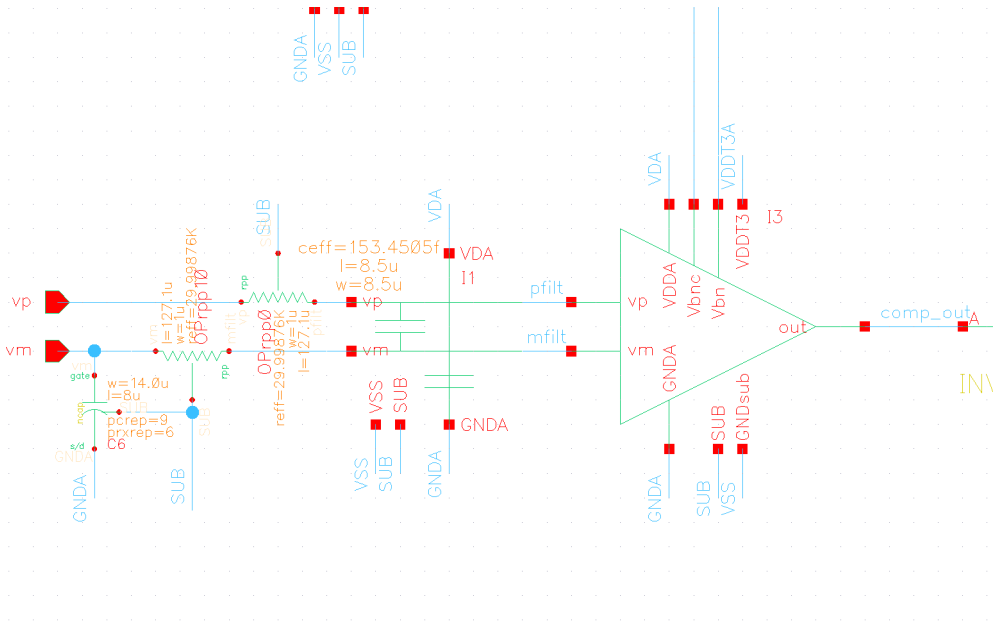

Figure 3.32: Comparator input with filter

Figure 3.32 shows the input of the comparator with an applied filter. In addition to the filter another capacitor is used in connection to GNDA. This is used to lower the supply voltage fluctuation caused by the abrupt change of supply current flow through the output stages which also affects the pre-amplification stage.

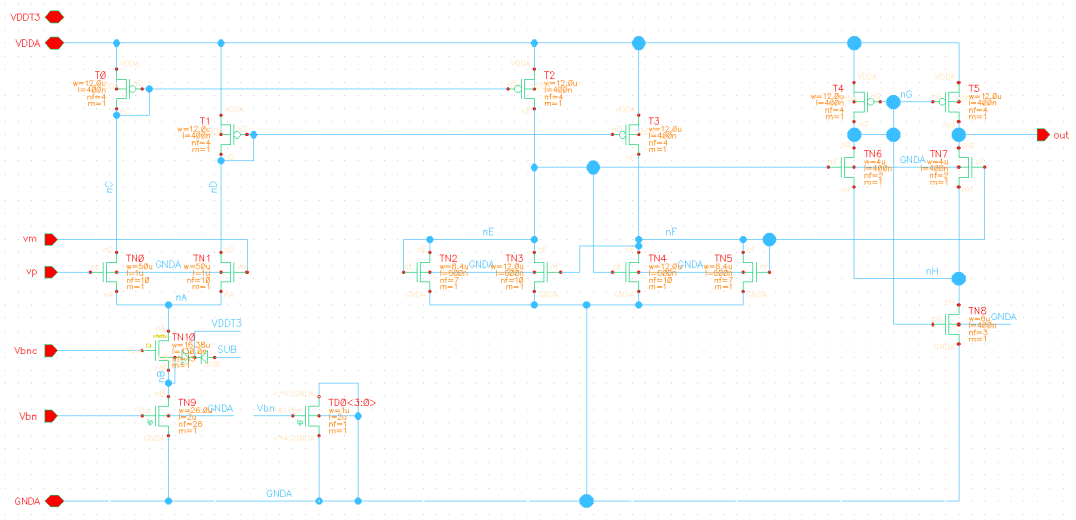

Figure 3.33: Comparator schematic

If the differential voltage V_m and V_p goes high then the drain voltage at the tail current source will follow. As it goes high this increases the current slightly due to channel length modulation $(1 + \lambda V_{DS})$. Now to make this bias current less dependent on V_{DS} we can use two techniques.

- Use large channel devices or
- Use Cascode technique

As shown in figure 3.33 cascode configuration has been used at the input. The purpose of the cascode is to get high gain, low noise and a stable operating point. In the previous chapter the comparator circuit was described in detail. The comparator circuit described in [4] has been used with minimal changes with respect to the input filter.

4 Layout

In the next few figures layout of the POR circuit is shown.

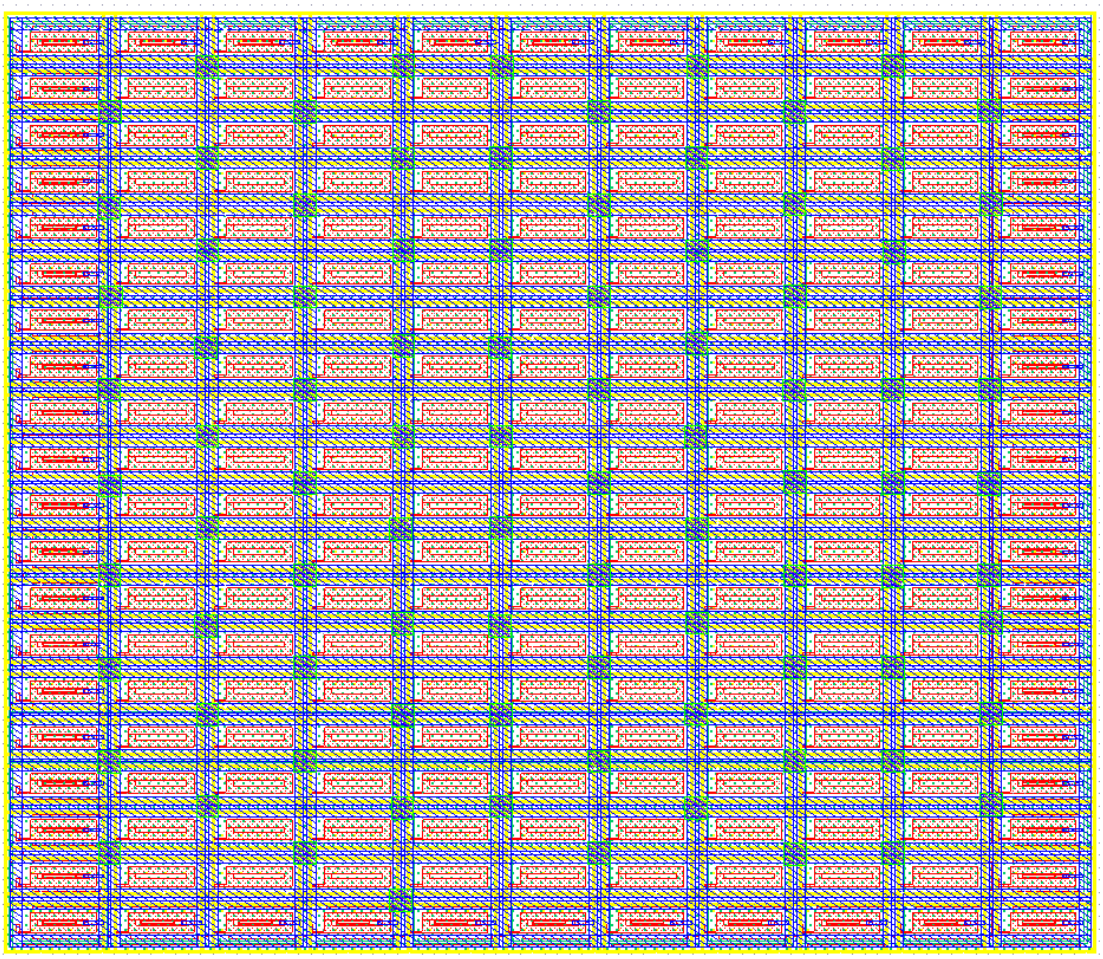

Figure 4.1: Layout of POR circuit(a)

Figure 4.1 corresponds to transistors Q_3 and Q_4 in figure 3.23. For transistor Q_3 multiplicity is 18 while for transistor Q_4 multiplicity is 144. Both transistors Q_3 and Q_4 are on the same voltage potential which is ground, and their drain, gates and bulk are shorted together. It can be seen from figure 4.1, the outer

consists of transistors placed in the same order but their drain source and gate all are shorted just to behave as a short circuit. These transistors are dummies which are placed to ensure that every core transistor has the same environment at all sides i.e. a transistor is sitting next to each transistor. This technique improves matching between transistors mismatch.

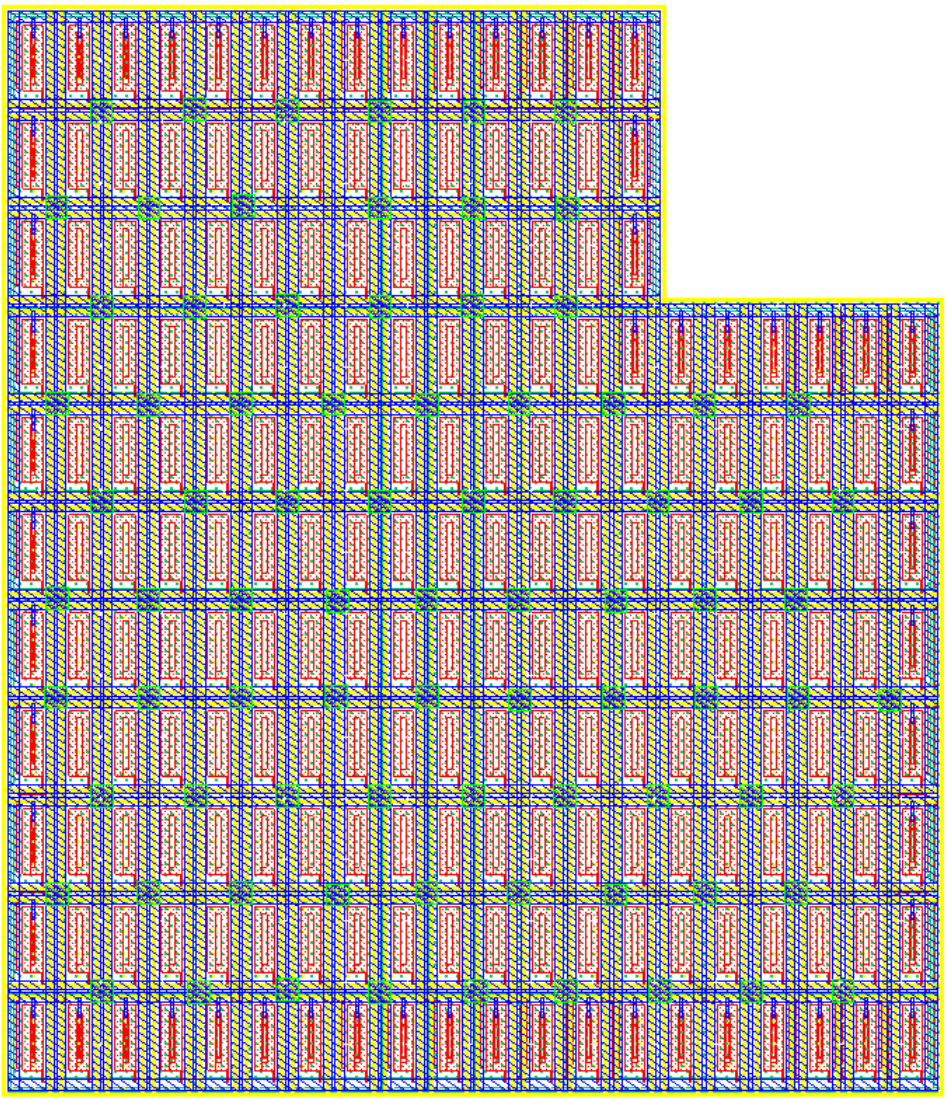

Figure 4.2: Layout of POR circuit(b)

Figure 4.2 corresponds to transistor Q_2 in figure 3.23. It has a multiplicity of 144. The reason for the different multiplicities between transistors Q3/Q4 and Q2 is to give different current densities in the two paths. The different current densities is the core requirement for the temperature stable switching behavior as

explained in section 2.2.1.

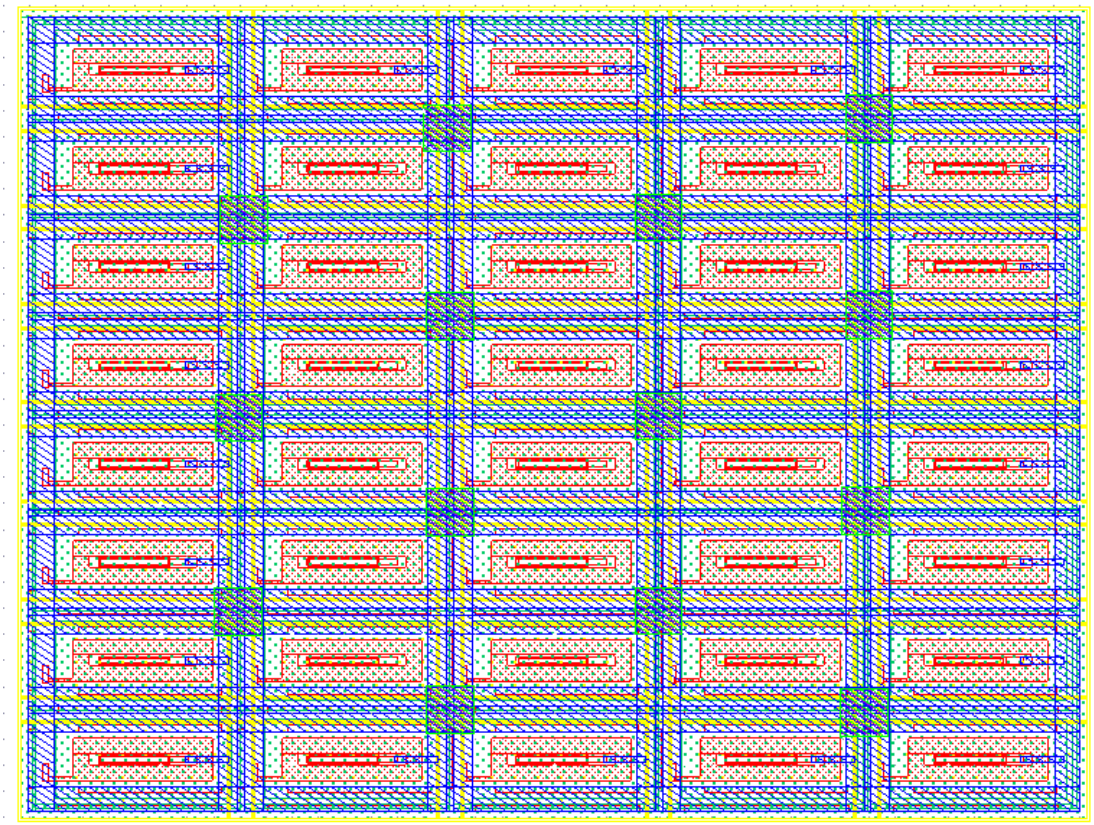

Figure 4.3: Layout of POR circuit(c)

4.3 corresponds to Q_1 in the figure 3.23. It has a multiplicity of 18. A radiation hard annular gate layout technique is used in which the gate is enclosed inside source [17]. By the annular gate technique, there is no FOX or STI oxide at the border of the transistor channel which could lead to increased leakage current with radiation dose. Major contribution towards Total Ionizing Dose (TID) induced current is caused by the Shallow Trench Isolation (STI) edge which lies between the source and the drain of a MOSFET. In the annular gate transistor technique, this edge is removed. The innermost layer is the drain terminal which is enclosed by the gate, the gate is then enclosed by the source terminal. In this way, the gate is fully enclosed by the drain and the source of the transistor leaving no edge.

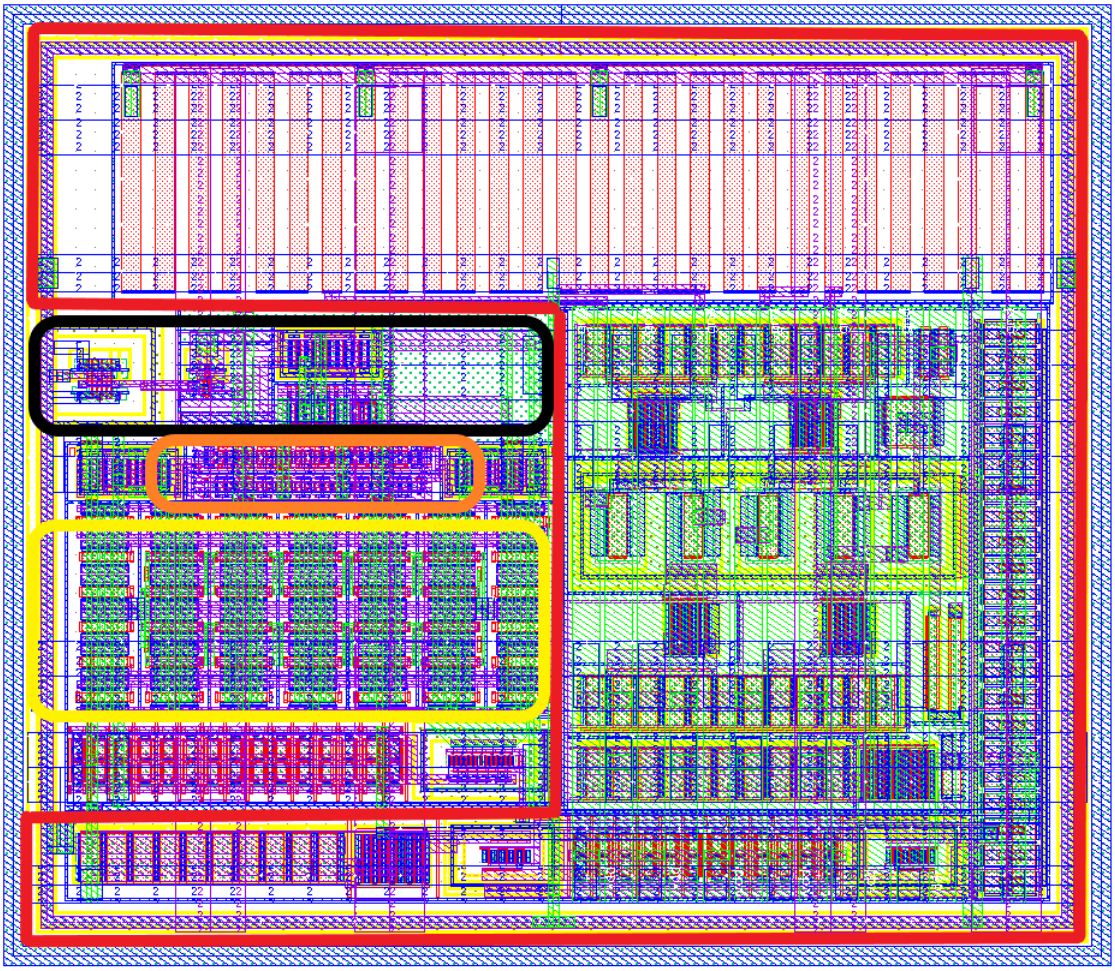

Figure 4.4: Layout of the comparator

Figure 4.4 shows layout for the comparator circuit. The red block is the biasing circuit. The yellow block is the input differential stage. The orange block corresponds to the decision circuit and the black block is the output buffer stage.

5 CAN ISO-11898:2015 and CANopen Standards

In this section first CAN ISO-11898:2015 is briefly summarized and then CANopen standard will be discussed. For detailed information please refer to both standards [18] and [19].

5.1 CAN ISO-11898:2015

CAN stands for *Controller area network* which is a serial bus communication protocol as shown in figure 5.1 where each node is connected to a single bus with 120Ω resistor termination to avoid reflections. Each node on the network can send data on the bus after arbitration and each node on the bus can receive after which it decides whether it is important to process or not. It was first developed by Robert Bosch GmbH in 1986 and then used by some major semiconductor companies like Philips and Intel. Since 1993 the CAN protocol and its extensions are defined in ISO-11898.

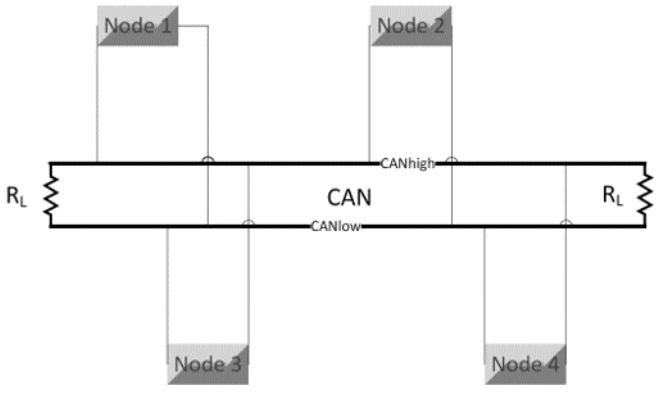

Figure 5.1: Controller area network

Initially CAN protocol had two versions.

- CAN 2.0A used 11-bit message identifier
- CAN 2.0B used 29-bit message identifier

Now CAN ISO-11898:2015 has 6 different parts.

- Part 1 defines the data link layer. which is then further divided into logical link (LLC) sub-layer and medium access control (MAC) sub-layer. Also the physical signalling (PHS) sublyer is defined in this part.
- Part 2 - Part 6 defines different implementation variants of physical medium attachment (PMA) and time triggered communication.

In this thesis, a brief introduction is given to the part 1. Some basic concepts and features of the CAN are described below.

5.1.1 Features and basic concepts

- Multi master priority based bus network
  Which means every node connected to the network can be a master node. At any given time only one node acts as master while other act as slaves.
- Non destructive message arbitration
  If a node loses arbitration the message is not destroyed instead it will wait until it gets the rights to write on the bus.
- Data is broadcasted to every node
  Every node broadcasts its data with no information about the receiver node so the message gets to every node connected to the network.
- Each node decides which messages are relevant to the process
  Each node has to decide whether the message is relevant and important to be processed or should be discarded.
- Robust error detection
  CAN provides several mechanisms for error detection which will be discussed later.

- Very flexible for configuration after deployment. E.g adding or removing new nodes
  Due to the fact that no receiver information is required e.g. node address etc and there is no point to point communication between different nodes. All the messages are broadcasted to every node. So, in case of the new node if it is not sending data in the future and just receiving then no message filtering is required for the previously installed nodes.

- Auto switch-off defective nodes
  CAN provides a mechanism in which nodes are put into different states according to the numbers of errors generated. In the extreme case a node is logically disconnected from the network automatically.

- Automatic retransmission
  If a node loses arbitration or errors are generated then the node will try to transmit until it gets the chance to write on the bus, the message is transmitted completely and correct reception is acknowledged.

- Differential signaling
  Due to the differential transmission electromagnetic emissions from the signal lines are limited and signal integrity is less influenced by surrounding electromagnetic fields.

- Data can be broadcasted as well as can be requested remotely
  Any node can broadcast its data at any time and can also send a remote transmission request.

As shown in figure 5.2 the CAN standard is defined for only last two layers of Open Systems Interconnection (OSI) model.

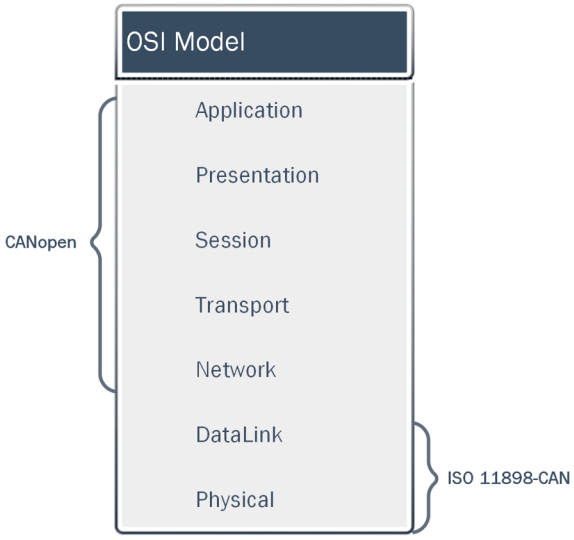

Figure 5.2: CAN OSI model

Detailed description of each layer is shown in the table form in figure 5.3

Physcial Layer	Datalink Layer	
PCS	MAC	LLC
• Bit encoding • Bit decoding • Synchronization	• Data encapsulation/de-capsulation • Frame coding • Medium access management • Error detection • Error signaling • Acknowledgment • Serialization • Deserialization	• Acceptance filtering • Overload notification • Recovery management

Figure 5.3: CAN layer Specification

Three different implementation options are available as per standard

- Classical CAN frame format is supported and the flexible data rate frame format is not tolerated
- Classical CAN frame format is supported but flexible data rate frame format is tolerated
- Both classical and flexible data rate frame format are supported

Here not tolerated means that if the flexible data frame format are used while it is not supported the generation of error frames will be caused. Two different frame formats are available:

- **Classical frame format:** 1 Mbit/s and 8 bytes of data per frame
- **Flexible frame format:** > 1 Mbit/s and up to 64 bytes of data per frame

Both of these frame formats can use either 11-bit identifier or 29-bit identifier. Structure of two different types of frames are shown in figure 5.4 and figure 5.5 respectively.

S O F	Arbitration field	Control Field	Data field	CRC field	E O F
	11 bits = Base or 29 bits = Extended	4 DLC bits and Some other Control bits	8 bytes	15 bits	

Figure 5.4: Classic base / extended frame format

S O F	Arbitration field	Control Field	Data field	CRC field	E O F
	11 bits = Base or 29 bits = Extended	4 DLC bits and Some other control bits	8 – 64 bytes	17 / 21 bits CRC + 4 bits stuff count	

Figure 5.5: FD base / extended frame format

There are some other bits for delimitation and control which are mentioned below.

- **Classic Base/ Extended Frame Format** SOF = 1 dominant bit, Arbitration field = 1 RTR bit / 3 bits (RTR,SRR,IDE), control field = 2 bits (ro,FDF), CRC = 1 bit delimiter, ACK = 1 bit delimiter, EOF = 7 recessive bits
- **FD Base/ Extended Frame Format** SOF = 1 dominant bit, Arbitration field = 1 RRS bit/ 3 bits (RRS,SRR,IDE), control field = 5 bits (IDE,FDF,res,BRS,ESI) / 4 bits (FDF,res,BRS,ESI), CRC = 1 bit delimiter, ACK = 1 bit delimiter, EOF = 7 recessive bits

Four different types of frames are used on CAN network.

- **Data Frame (DF):** Used to carry data from a transmitter to all receivers
- **Remote Frame (RF):** Frame used by a node to request data from some other node using the same identifier
- **Error Frame (EF):** Transmitted by any node in case of a detected bus error
- **Overflow Frame (OF):** Used to provide some delay in between DF and RF
  - Data frames and remote frames shall arbitrate for access to the bus
  - Conflict is resolved by arbitration, a message with the highest priority gets access. In case of same ID DF always wins
  - Data frames and remote frames shall be separated from preceding frames by inter-frame space i.e. 3 bits
  - Frames marked as corrupted are retransmitted typically 17 upto 31 nominal bit times
  - If a frame is not acknowledged it is marked as corrupted
  - Depending on the number of error counts a node is put in error active, error passive and bus off state (logically disconnected)

MAC sublayer provides the following 5 error checks.

- Bus monitoring
- Stuff rule check
- Frame check
- CRC check
- ACK check

Purpose of fault confinement is to make sure bus is available all the time irrespective of faulty nodes.

- To make distinction between permanent and temporary failures.

- Switching off faulty nodes logically so that they are not allowed to send and receive data.

The fault confinement block categorizes the nodes with respect to the number of errors they are generating or the number of successful message transmission or reception events. CAN nodes can be in one of the following three states mentioned below:

- Error active
  - Transmit/receive error counter < 127
- Error passive
  - Transmit/receive error counter > 127
- Bus-off state
  - Transmit error counter > 255
  - The node returns to the active state upon restart/normal mode request and 128 occurrences of 11 consecutive recessive bits

Figure 5.6 shows the way how a CAN node interacts with other nodes on the network depending on its error status.

Node status	Send	Receive	Ack	Error frame
Error active	✓	✓	✓	6 consecutive dominant bits
Error passive	✓ (wait time)	✓	✓	6 consecutive recessive bits
Bus-off	×	Implementation dependent	×	×

Figure 5.6: Fault confinement status and interaction

In figure 5.6 wait time for a passive node means it has to wait for 8-bit times before starting a new transmission.

5.2 CANopen Standard

CANopen is a device and manufacturer independent standard for communication between the nodes on a CAN network. CANopen implements the application

layer in the OSI model while there is no need for the network, transport and other OSI layers. CANopen meets the physical and the data link layer requirements defined for CAN ISO-11898:2015 standard. Using the CANopen standard the number of devices on the CAN network are limited to 127 because of the fact that it allocates 7 bits of the 11 bit message identifier to address each node on the network. By using predefined identifiers CANopen reduces the communication overhead and simplifies filtering for the nodes. Using CANopen the CAN network can be operated in a synchronized way.

In the following, the need for the standardization of higher level protocols is discussed.If a CAN network is implemented all communication nodes have to agree on a set of definitions at the application layer.
This should become clear by the following examples

- Usually the CAN network node is controlled by a CPU or a micro-controller and interacts with an embedded system or a user interface on the other side.
- For every node it has to be clearly defined which messages should be processed and which needs to be discarded.
- A CAN node might need a firmware upgrade applied from the remote.
- With a large number of CAN devices available in the market compatibility has to be assured.
- A node should be switched off logically when node operation is not required.
- Node messages should be send e.g. in a synchronous way, event driven etc.
- Definitions on how devices are configured, synchronised and data is transferred.

To solve all the raised issues and to practically use a network to send data one has to define some protocol at the application layer so the devices communicate efficiently. CANopen provides a generalized model at the application layer which is clearly developed and defined making it easier for the users to implement a CAN network.

CANopen offers two different modes of transmission

1. Synchronous Transmission

2. Event-Driven Transmission

There are three different modes of message triggering

1. Event and Time Driven
    - Message transmission is started whenever there is some specified event or when a certain time has passed.

2. Remotely Requested
    - Message transmission starts on receiving Remote Transmission Request (RTR). RTR frame is same as data frame except there is no data field.

3. Synchronously Triggered
    - After transmission of Synchronization Object (SYNC) or a number of SYNCs.

Object Dictionary

In a CANopen network, devices communicate with each other using a predefined standard set of information which are called objects. Information stored in these objects in most cases is passed on to other nodes just like a normal CAN message which was defined in figure 5.4 or figure 5.5. However, CANopen is defined and accustomed to the classical frame format shown in figure 5.4. CANopen objects can be compared to a variable or a set of variables (array) as used in high level programming languages to store information. This data stored in these variables is called from the memory. In the same way an object dictionary is defined in CANopen which stores information about all the available objects. Assume for example a machine with an LCD display connected to a CAN network which has the ability to change his display brightness remotely by CANopen messages. In this case an object would be defined which holds all information about the LCD brightness.

Index	16-bit (8-bit sub)
Object type	Variable, array, string etc
Name	Name of the object
Data type	Integer, float, unsigned etc
Access rights	Rw,ro,wo
Default value	-

Figure 5.7: Object information listed in the object dictionary

Figure 5.7 shows the information which is listed for each object in the object dictionary. A complete overview of how an object dictionary looks like is given on page 148 table 74 of the CANopen standard [19].
An object is addressed or accessed by using a 16-bit index while each object can have another 8-bits sub-index. As a result an object dictionary can have a maximum of 65,536 objects. Information in these objects can be stored using data types defined in CANopen standard e.g. boolean, integer, floating point and compound data types like arrays etc. Figure 5.8 shows the CANopen device model. The object dictionary contains objects which have information about device manufacturer, model, device type etc. On the application side different application objects may be defined to serve a dedicated function for example one such function could be the control of the LCD display brightness as previously described. This application object maps to a specific index of 16-bit. In the object dictionary this 16-bit index refers to the address of one of the communication objects mentioned below. As shown in figure 5.9 this object has a 4-bit function code to define its type and priority and a 7-bit node ID.

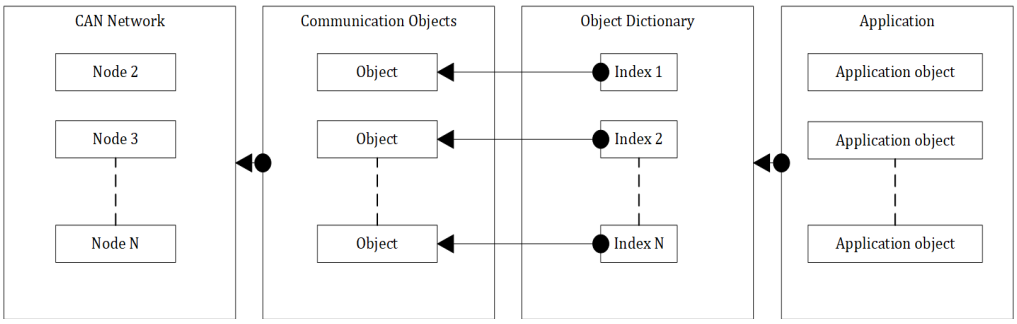

Figure 5.8: CANopen device model

There are 6 different types of communication objects defined in CANopen standard.

1. Process Data Objects (PDO)

2. Service Data Objects (SDO)

3. Synchronization Object (SYNC)

4. Time Stamp Object (TIME)

5. Emergency Object (EMCY)

6. Network Management (NMT)

PDOs and SDOs can be used to access the object dictionary. Each object type has different priority. If two CANopen devices want to start communication then the device which wants to send a high priority object wins. As shown in figure 5.9 the 11-bit message identifier of a CAN bus is broken down into two pieces in a CANopen network.

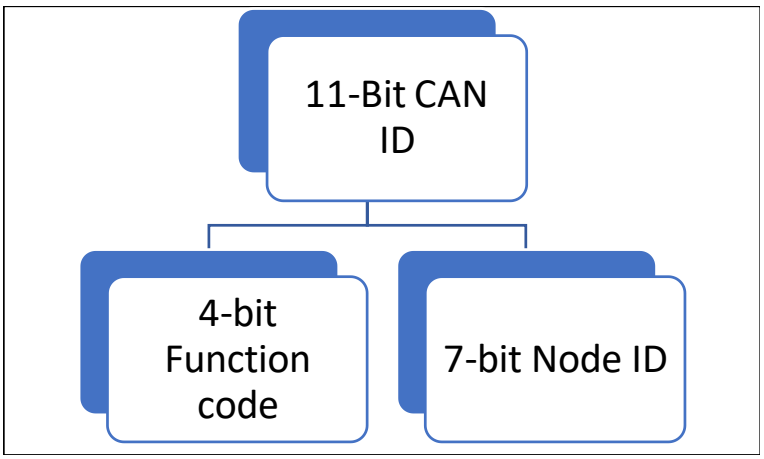

Figure 5.9: COB ID

So, the first 4-bits corresponds to function code and the next 7-bits identify a node. These 4-bits are used to identify which communication type of object is referred to and its priority. Complete format of CANopen message is the same as defined in figure 5.4. System designers of the CANopen network must take into account that

- All the nodes are operating at the same bit rate
- Same node ID is not assigned to more than one nodes

There are three different communication protocol models defined for CANopen standard.

- Master / Slave
- Client / Server
- Producer / Consumer

Master / Slave configuration

In a master/slave configuration, the single CANopen device in the network serves as a master while all other devices serve as slaves. This master device sends a request and depending upon whether it is a confirmed or an unconfirmed service the slave devices respond or just execute the command.

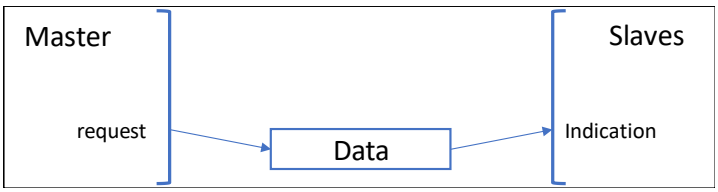

Figure 5.10: Master / Slave unconfirmed

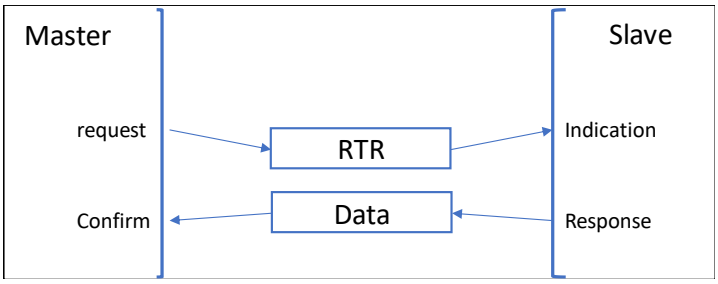

Figure 5.11: Master / Slave confirmed

Figure 5.10 and 5.11 shows the master / slave communication scheme. In case of a confirmed transmission the master sends a request and the slave responds with the data.

Client / Server configuration

The Client / Server model is used for a single client and a single server. When a client issues a request which can be an upload or download request, the server performs the task accordingly and responds as soon as the task has been executed.

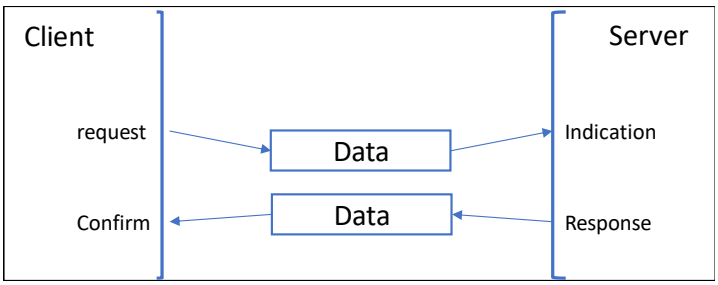

Figure 5.12: Client / Server

Producer / Consumer or Push / Pull model

The Push model is similar to Master / Slave approach with an unconfirmed protocol. The only difference is the number of producers in the network which can

be more than a single one.
The Pull model is similar to Master / Slave approach with a confirmed protocol but with a more than one consumer and the RTR flag is generated by the consumers while response is generated by the producers.

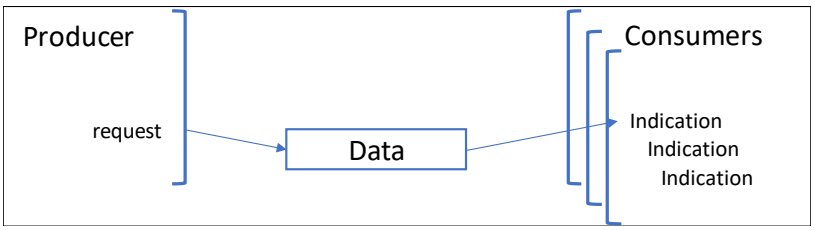

Figure 5.13: Push model

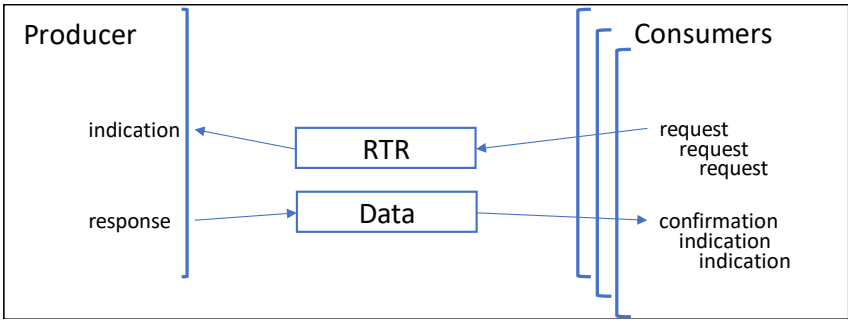

Figure 5.14: Pull Model

In section 5.2 there are six different CANopen objects mentioned. Below are further details about each one of them.

5.2.1 Process Data Objects (PDO)

Process data objects are general purpose data transfer objects. As is indicated from the naming they are used for data that is changing over time e.g data from sensors or some other input/output units like motors, encoders etc. They have the following characteristics.

- They are used to transfer real-time data with no protocol overhead.
- PDOs are defined in the object dictionary and they provide interface for the application objects.
- Number and length of PDO is application dependent.

- PDOs are transferred using Producer/Consumer model.

- PDO write is executed according to a push model while PDO read is based on the pull model.

- Data from multiple data objects can be combined into one PDO however an SDO can access one object at any given time that means using a single PDO data from multiple objects can be sent.

- There are two types of PDO i.e. Transmit-PDO and Receive-PDO. Transmit-PDO corresponds to data coming from the producer node while Receive-PDO corresponds to data received by the consumer node.

- For PDOs two different parameters must be defined in the object dictionary which are configuration and mapping. The configuration parameters define how the transmission is initiated, the COB-ID, and the event timer, while the mapping parameter defines which of the objects from the object dictionary get into a specific PDO. PDO mapping is shown in figure 5.15.

- There are three different options available for transmission which are time driven, event driven or synchronised.

- The data field of a PDO can be 0 to 8 bytes long. As specified in 5.4

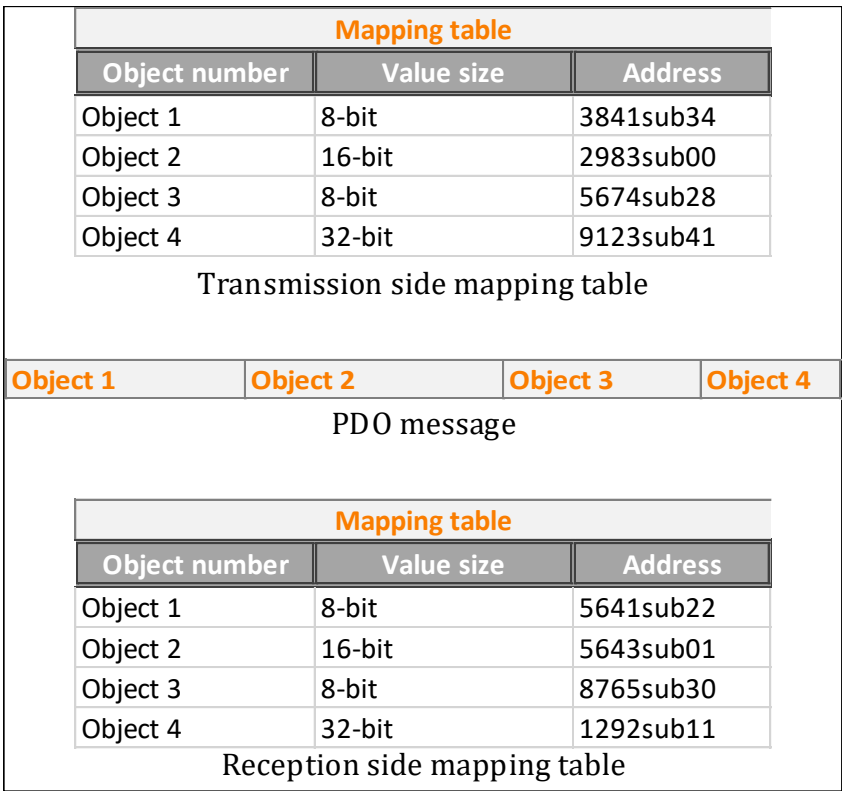

Figure 5.15: PDO mapping

5.2.2 Service Data Objects (SDO)

Service data objects provide direct access to objects in the object dictionary. Information stored in these objects can be written, read and modified using SDOs. The Node which handles the data is called client while the node whose object dictionary is accessed and modified/configured is called server. In the following, the characteristics of SDOs are listed.

- SDOs are used to configure CANopen devices during the initialization phase and also during operation.
- SDOs use the client/server model mentioned before.
- SDO communication requires an initialization phase in which client and server prepare themselves for data transfer.
- SDOs Provide a way for peer-to-peer communication in CANopen standard.

- CANopen standard defines that each node on the network must implement a server to allow access to its object dictionary for modifications and configuration.

There are three different ways data can be transferred using SDOs. Based on SDO communication a virtually unlimited size of data can be transferred.

1. Expedited transfer
2. Segmented transfer
3. Block transfer

Expedited transfer

The expedited transfer is carried out during the initialization phase when two nodes agree to start peer-to-peer communication. Using expedited transfer only 4-bytes of actual data transfer is possible while the other 4 bytes of the data field is used for other control information. Figure 5.16 shows the frame format for expedited data transfer. The first byte corresponds to the specifier which gives information about the number of data bytes and the type of transfer etc. Figure 5.17 shows detailed information about the specifier byte. The first three bits named as client specifier provide the information about the operation being performed i.e. abort message or read/write. The fourth bit is reserved. The fifth and sixth bits indicate the number of bytes in the data field which do not contain actual data. The seventh bit differentiates between expedited and segmented transfer and the last bit defines whether the data size is specified in the fifth and sixth bit if it is specified in the data field.

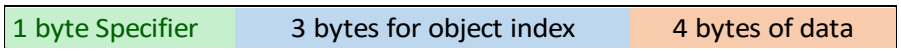

Figure 5.16: SDO frame format

Client command specifier	Reserved	Number of bytes with no data	Espedited transfer ??	Data size
3bits	1bit	2bits	1bit	1bit

Figure 5.17: SDO specifier byte

Segmented transfer

The segmented transfer is used when the whole data does not fit into 4 bytes available in the data field. If more than 4 bytes of data are needed to be transferred then a segmented transfer is required where each segment consists of 7 data bytes. Initialization is required to be done only once. When the segmented transfer is chosen then the 4-bytes of data field in the initialization frame is also used to specify the length of the data segments to be transmitted. The segmented transfer is done using SDO segment download and SDO segment upload service.

Block transfer

In the new version 4.2.0 of CANopen standard a new transfer mode is proposed which is named block transfer. It operates similar to segmented transfer with the difference that each segment is not acknowledged individually but in blocks. In addition the CRC checksum is run over the entire block to maximise data transfer and to reduce the protocol overhead. Each block can consist of a maximum of 127 segments.

5.2.3 Other CANopen Objects

There are 4 other type of CANopen objects for network management to assure seamless communication.

Synchronization Object (SYNC)

The Synchronization object is used to synchronise CANopen devices across the network. It is broadcasted periodically. The time period after which SYNC object is sent again is defined in the parameter of object "communication cycle period". To make sure SYNC objects get access to the bus they are given a very high priority. The SYNC object is communicated using producer/consumer push model.

Time Stamp Object (TIME)

This object broadcasts the time stamp across the network. There can be some jitter and latency for this object. When TIME object is received by any node it adjusts its local clock with the network global time.

Emergency Object (EMCY)

The emergency object is sent when a CANopen node detects an internal error e.g low/high voltage/current, high operating temperature etc. For any specific error, only one EMCY object is sent. Emergency objects are sent with 8 data bytes. This is an optional object. If this is implemented in a CANopen node then it should support at-least two states, error free and error accured state.

Network Management (NMT)

Network management objects are used to manage the CANopen network. They are used to logically turn OFF/ON any node. In a CANopen network, any node can be in 4 different states. They have the highest priority with COB-ID 0 and are compulsory objects in a CANopen network. The NMT communication follows a master/slave protocol. There is only one master and all other devices are slaves.

NMT communication is processed in four states.

1. Initialization
2. Pre-operational
3. Operational
4. Stop

Initialization state

Whenever a node is turned ON or a hard reset is applied a CANopen node starts in this state. The node resets the application and communication profiles. After reset is finished a start-up message is sent and the node switches to the pre-operational state.

Pre-operational

In this state CANopen devices are configured. PDOs can not be transmitted in this state while SDOs and other NMT objects can be transmitted.

Operational

Operational state is when a node is working properly and is able to transmit PDOs.

Stopped

Only node guarding and heartbeat messages can be sent in this state.

Figure 5.18 and 5.19 shows the priorities of CANopen objects and their function codes. To use CANopen on any device on-chip RAM and ROM are required whose size are dependent on object dictionary size and overall functionality.

Communication Object	Function Code	CAN-ID
NMT	0000	0
SYNC	0001	128
TIME	0010	256

Figure 5.18: CAN objects function codes and priority(a)

COB	Function code	CAN-ID
EMCY	0001	129-255
PDO1 (tx)	0011	385-511
PDO1 (rx)	0100	513-639
PDO2 (tx)	0101	641-767
PDO2 (rx)	0110	769-895
PDO3 (tx)	0111	897-1023
PDO3 (rx)	1000	1025-1151
PDO4 (tx)	1001	1153-1279
PDO4 (rx)	1010	1281-1407
SDO (tx)	1011	1409-1535
SDO (rx)	1100	1537-1663
NMT error control	1110	1793-1919

Figure 5.19: CAN objects function codes and priority(b)

5.3 Canakari Design

The Canakari design has been chosen for the implementation of the CAN protocol unit in the DCS controller chip. A block diagram for the Canakari design is shown in figure 5.20. It consists of 7 main blocks at the top level hierarchy.

1. Medium access control
2. I/O control unit
3. Timing control
4. Logical link control
5. Fault confinement
6. Interrupt control
7. Clock Pre-scaler

The core of the design is developed and proposed in [20]. After the initial design several modifications have been introduced afterwards. For example The Clock Pre-scaler block and the interrupt control block were added. The tasks of the Medium access control block and the logical link control are defined in table 5.3.

A test-bench has been written to verify the CAN protocol unit and especially the introduced design modifications.. This test-bench is used to simulate and verify the Canakari design in behavioural simulations. In the test-bench a pattern generator package is defined to create a correct CAN frame which is then compared with the actual frame generated by the Canakari controller. This pattern generator generates a correct frame for both transmitting and receiving nodes in a CAN network.

For the transmission side, the test bench generates an acknowledgement if the message is generated correctly. If there is a mismatch between the two frames where one is generated by the Canakari controller and the other one by the test pattern generator then an error is generated.

For the reception side, an acknowledgement is generated by the Canakari controller if the message is received and de-capsulated correctly.

5.3.1 Behavioural Simulation

Figure 5.21 shows the simulation results when the canakari controller acts as a transmitting node. There is no mismatch between waveforms t_x, r_x and tx_{pg}. At

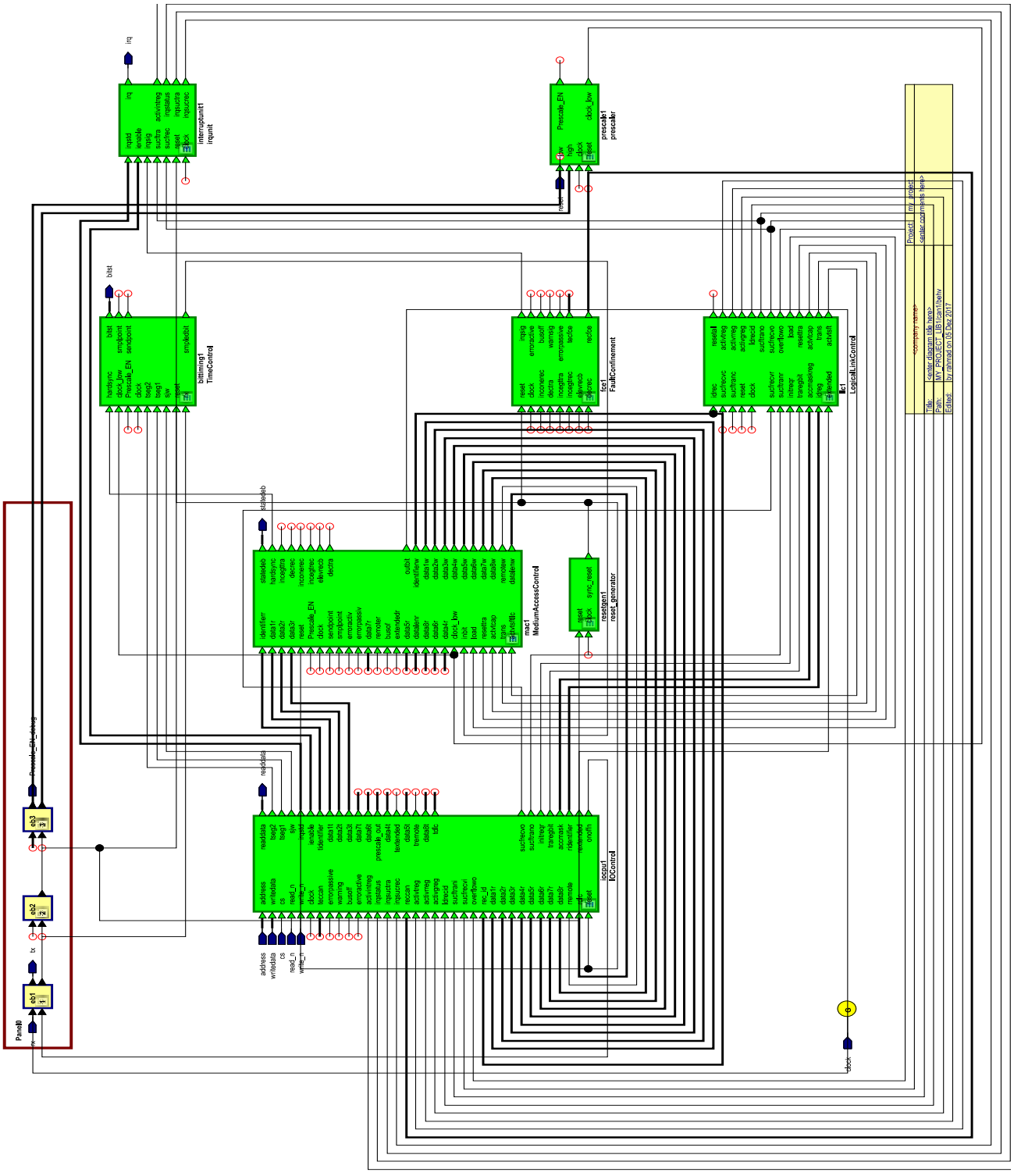

Figure 5.20: Canakari block diagram

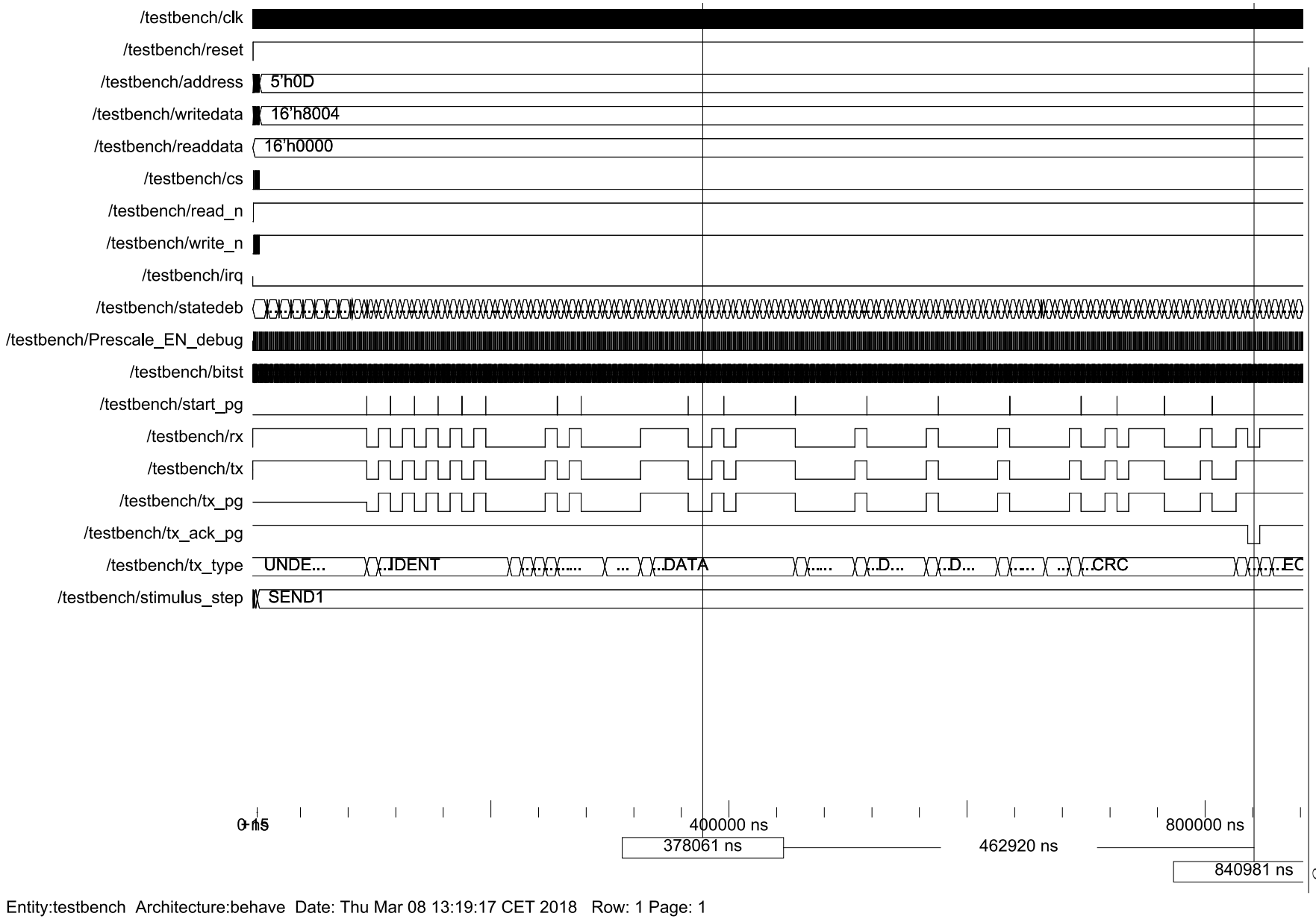

Figure 5.21: Canakari transmission mode

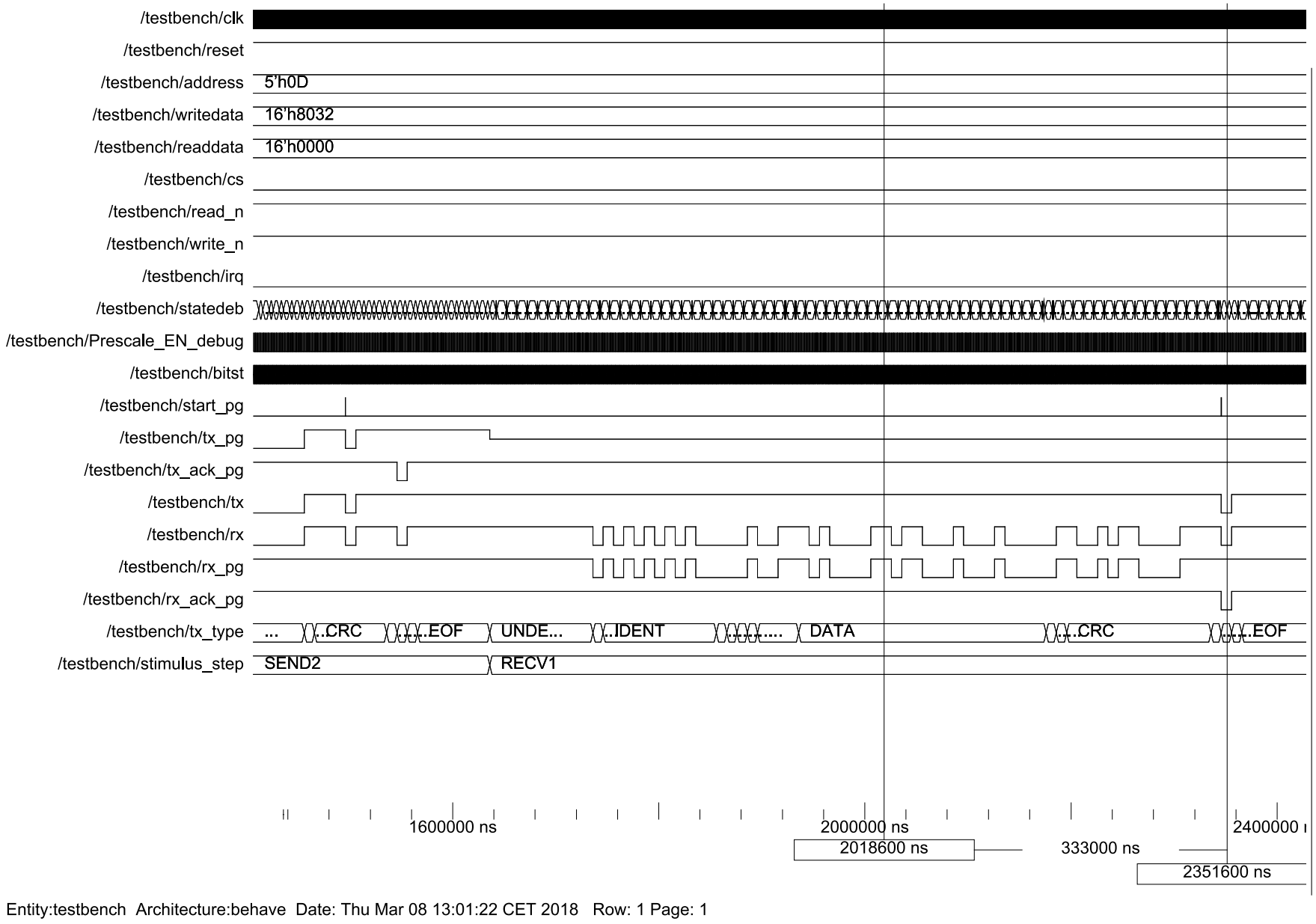

Figure 5.22: Canakari reception mode

point 840981ns an acknowledgement bit is generated by the receiver to indicate correct reception.

Figure 5.22 shows the simulation result when the Canakari node acts as a receiver. Since there is no mismatch between the two waveforms r_x and rx_{pg} where one is generated by the pattern generator while the other one is generated by the Canakari. A point 2351600ns an acknowledgement bit is generated by the Canakari controller to indicate correct reception.

Figure 5.23 shows the case when there is some CRC error generated because the data is corrupted during transmission. At the marker placed at 1210279ns it can be seen that a dominant logic bit is missing in the data field of the CAN frame generated by the Canakari controller while it is generated by the pattern generator. t_x and tx_{pg} are the CAN frames from the Canakari and the pattern generator respectively. A mismatch is seen between the CRC code generated at the transmitting and the receiving nodes. This causes a CRC error which is indicated by sending 6 dominant bits after the acknowledgement bit.

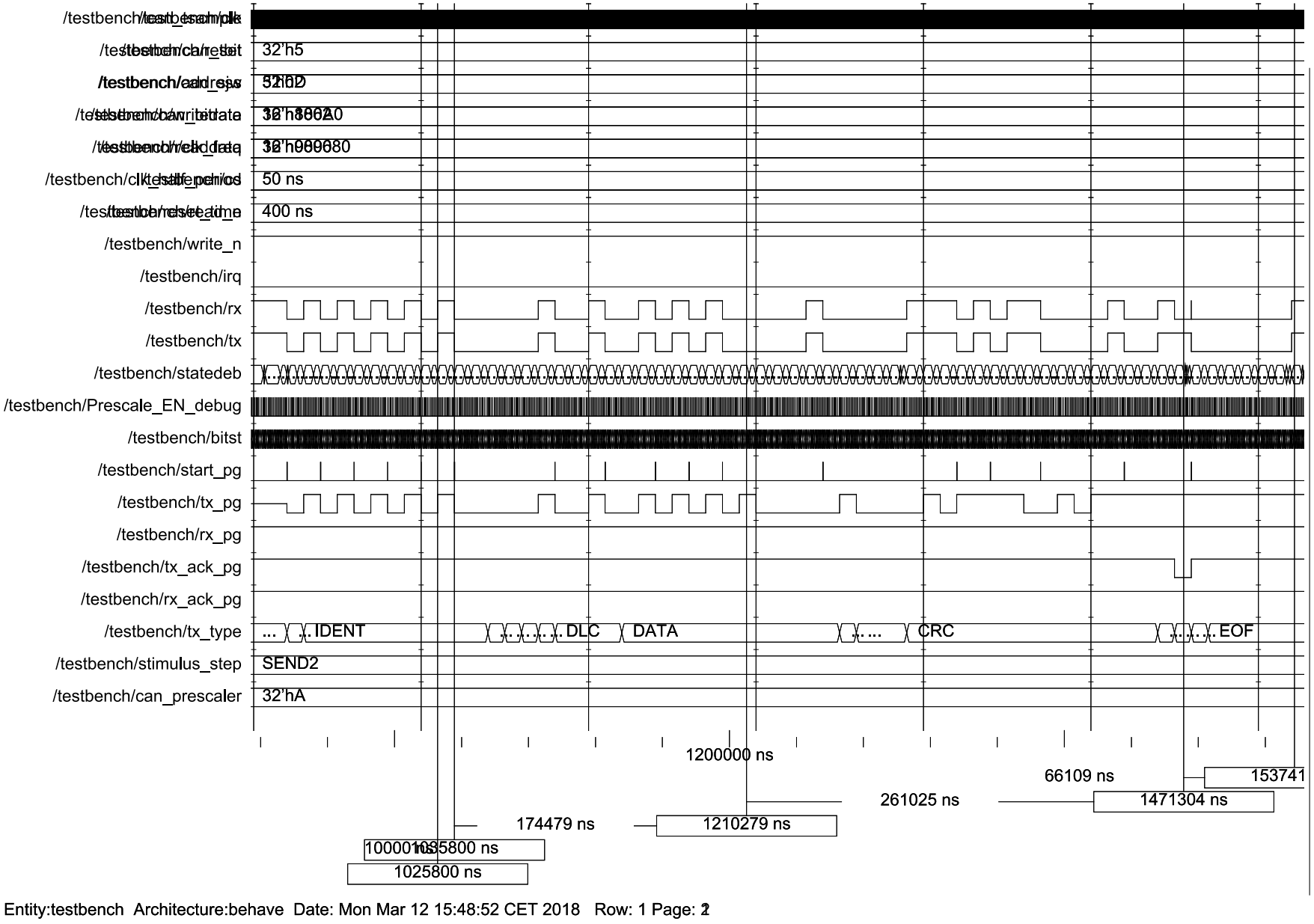

Figure 5.23: Canakari CRC error for corrupt data

6 Summary and Future Work

This master thesis was a contribution towards the development of a prototype for the detector control system of the ATLAS pixel detector. For this upgrade on-chip shunt, Linear regulator and a Power-On-Reset circuit has been designed using Globelfoundaries(former IBM) 130nm CMOS technology. The DCS system inlcudes three main parts as shown in figure 1.3. The Shunt/Linear regulators and the Power-On-Reset circuit designed in this master thesis will be used for prototyping the DCS chip allocated for each module inside the detector. The DCS controller is the communication bridge between the DCS chip and the DCS computer. For this DCS controller there must be on-chip bridge logic for communication between CAN node and I^2C master node so that the two different bus systems can communicate. For the DCS controller an already built CAN node is available which is the Canakari design implemented in [20] but this design needs to be verified first. A sophisticated test-bench is needed to verify the complete functionality. After that a bridge logic is required to be implemented for communication between CAN node and I^2C master node. On top level there is a need to develop some communication protocol at application layer for communication between different DCS controllers and DCS computer. For this purpose CANopen standard implementation is required to be investigated.

Bibliography

[1] K. Kuijk, "A precision reference voltage source," *IEEE Journal of Solid-State Circuits*, vol. 8, no. 8, pp. 222–226, 1973.

[2] T. Tanzawa, "A process- and temperature-tolerant power-on reset circuit with a flexible detection level higher than the bandgap voltage," *Proceedings - IEEE International Symposium on Circuits and Systems*, pp. 2302–2305, 2008.

[3] N. Lehmann, M. Karagounis, S. Kersten, and C. Zeitnitz, "Development of a Detector Control System for the ATLAS Pixel detector in the HL-LHC," *Journal of Instrumentation*, vol. 11, no. 11, pp. 1–6, 2016.

[4] N. Lehmann, "Description and Manual for the PSPPv3 Chip," 2017.

[5] M. Čermák, "Design of low-dropout voltage regulator," 2016.

[6] M. Bochenek, "Development of radiation resistant CMOS integrated circuits for the power distribution system in the upgraded ATLAS Semiconductor Tracker," Ph.D. dissertation, 2012.

[7] K.-H. Chen, *Power Management Techniques for Integrated Circuit Design*, chen2016, 2017.

[8] M. A. Karagounis, "Analog Integrated CMOS Circuits for the Readout and Powering of Highly Segmented Detectors in Particle Physics Applications," Ph.D. dissertation, 2010.

[9] V. L. a. A. V. Vidyapeetham, "Zener Diode as Voltage Regulator," 2012. [Online]. Available: vlab.amrita.edu,.(2012).ZenerDiodeasVoltageRegulator. Retrieved15January2018,fromvlab.amrita.edu/?sub=1{&}brch=282{&} sim=1207{&}cnt=1

[10] U. V. Wali, R. N. Pal, and B. Chatterjee, "On the Modified Nodal Approach to Network Analysis," *Proceedings of the IEEE*, vol. 73, no. 3, pp. 485–487, 1985.

[11] B. Razavi, *Behzad Razavi Design of Analog CMOS Integrated Circuits*, 2001.

[12] V. K. Peddinti, "ELE539 Project Band-Gap Reference Circuit."

[13] A. J. Annema, "Low-power bandgap references featuring DTMOSTs," *European Solid-State Circuits Conference*, vol. 34, no. 7, pp. 116–119, 1998.

[14] T. Blalack and B. A. Wooley, "The effects of switching noise on an oversampling A/D converter," *Solid-State Circuits Conference, 1995. Digest of Technical Papers. 41st ISSCC, 1995 IEEE International*, vol. 29, no. 3, pp. 200–201, 1995.

[15] R. J. Baker, *CMOS Circuit Design, Layout, and Simulation*, baker2012, 2010.

[16] P. Twepp, N. Lehmann, P. Bergmann, S. Kersten, P. Kind, Y. Narbutt, J. Schick, C. Zeitnitz, R. Ahmad, T. Fröse, and M. Karagounis, "PoS (TWEPP-17) 026," no. September 2017, pp. 0–4.

[17] A. J. Womac, "The Characterization of a CMOS Radiation Hardened-by-Design Circuit Technique," *Masters Theses*, 2013. [Online]. Available: http://trace.tennessee.edu/utk{_}gradthes/2479{%}5Cnhttp://trace.tennessee.edu/utk{_}gradthes/2479/

[18] International Standard Organization, "ISO 11898:2015 Road Vehicles-Controller Area Network (CAN)," 2017.

[19] C. i. A. (CIA), "CANopen application layer and communication profile, version 4.02. CiA (CAN in Automation)," no. February, 2002.

[20] M. A. Karagounis, "Design eines CAN Controllers mit VHDL und SpecCharts," 2000.